



TGD N-Channel Enhancement Mode Power MOSFET

Description

The TGD1579C uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

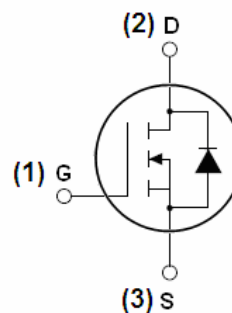
- $V_{DS} = 150V, I_D = 79A$
 $R_{DS(ON)} < 13m\Omega @ V_{GS} = 10V$ (Typ: 11m Ω)
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

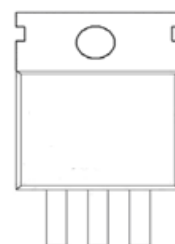
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

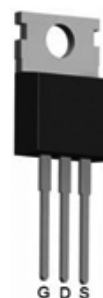
100% ΔV_{DS} TESTED!



Schematic diagram



pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
1579C	1579C	TO-220-3L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	79	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D (100^\circ\text{C})$	56	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	310	W
Derating factor		2.07	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note 5)	E_{AS}	480	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.48	$^{\circ}\text{C/W}$
--	-----------------	------	----------------------

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

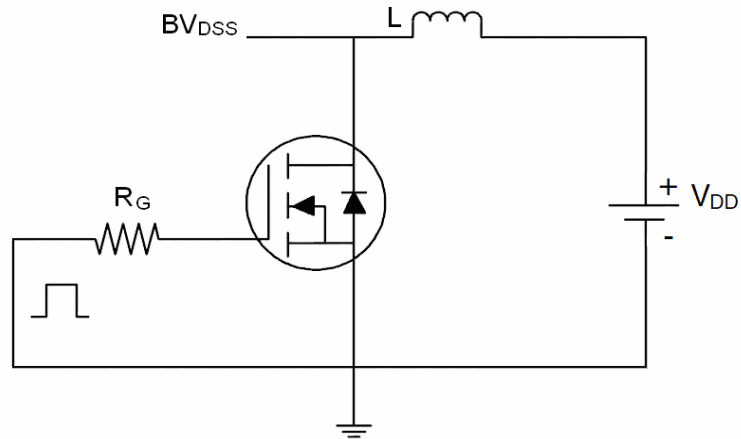
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	150	160	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3.1	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	11	13	mΩ
Forward Transconductance	g _{FS}	V _{DS} =15V, I _D =40A	120	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	7200	-	PF
Output Capacitance	C _{OSS}		-	463	-	PF
Reverse Transfer Capacitance	C _{RSS}		-	352	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	VDD=30V, ID=2A, RL=15Ω, RG=2.5Ω, VGS=10V	-	40	-	nS
Turn-on Rise Time	t _r		-	38	-	nS
Turn-Off Delay Time	t _{d(off)}		-	140	-	nS
Turn-Off Fall Time	t _f		-	60	-	nS
Total Gate Charge	Q _g	ID=30A, VDD=30V, VGS=10V	-	160	-	nC
Gate-Source Charge	Q _{gs}		-	31	-	nC
Gate-Drain Charge	Q _{gd}		-	64	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =40A	-	0.82	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	79	A
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 40A di/dt = 100A/μs ^(Note3)	-	42	-	nS
Reverse Recovery Charge	Q _{rr}		-	69	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

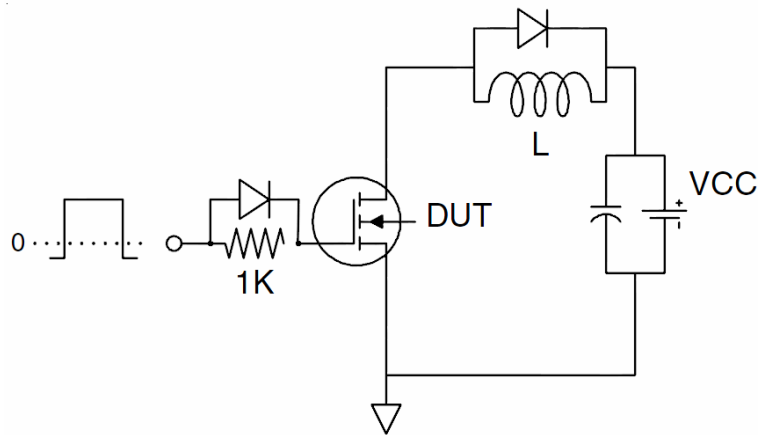
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

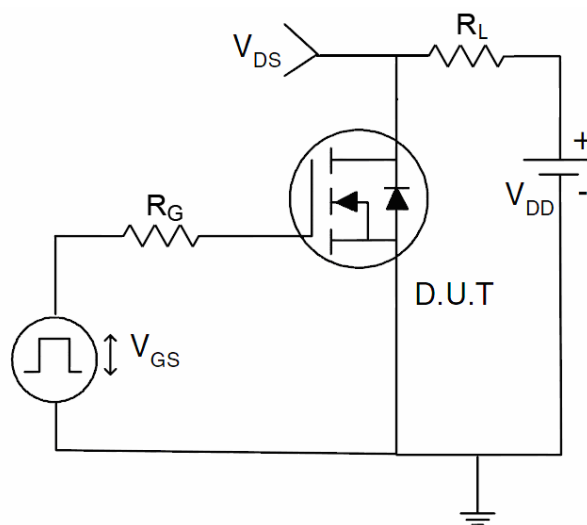
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

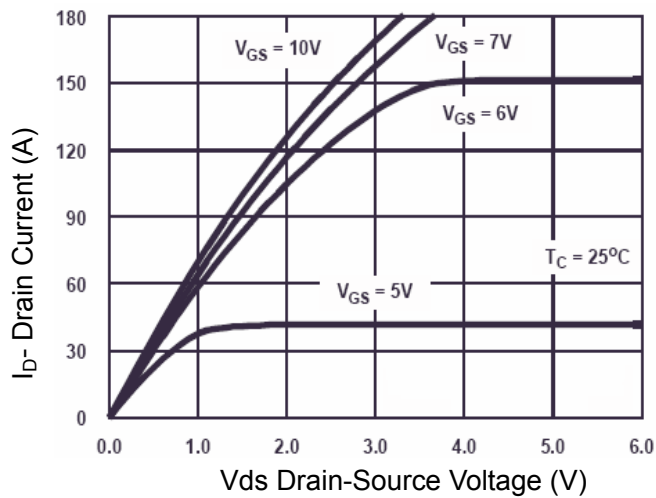


Figure 1 Output Characteristics

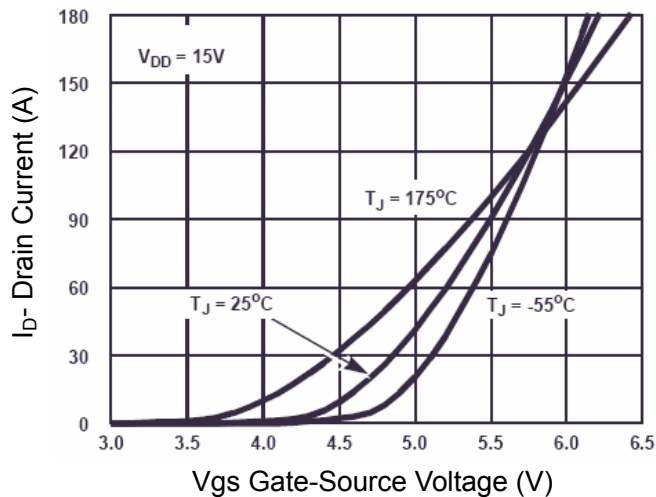


Figure 2 Transfer Characteristics

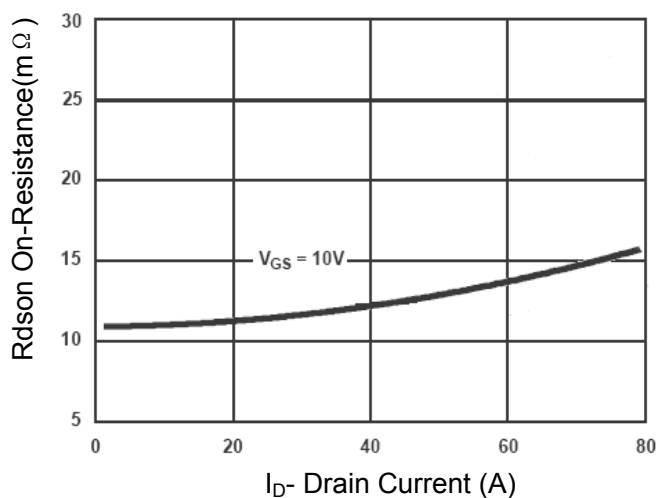


Figure 3 $R_{DS(on)}$ - Drain Current

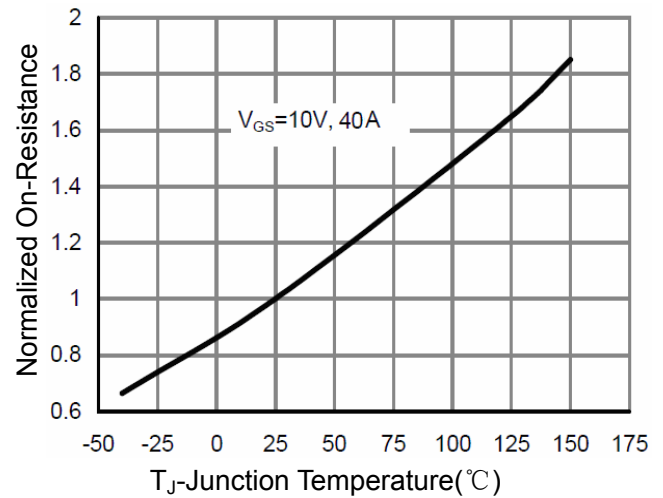


Figure 4 $R_{DS(on)}$ -Junction Temperature

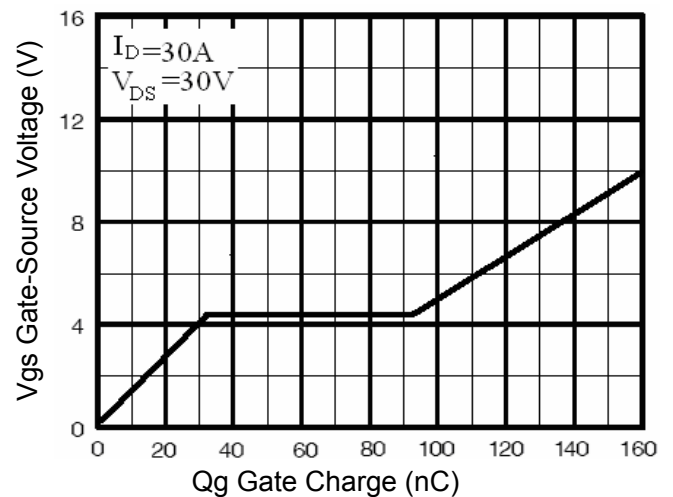


Figure 5 Gate Charge

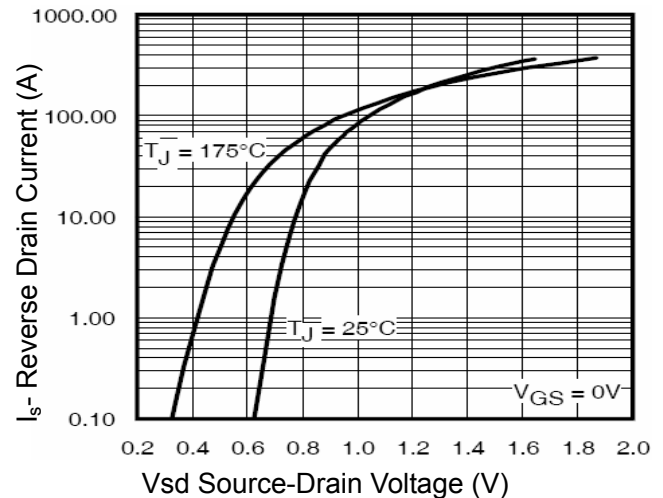


Figure 6 Source- Drain Diode Forward

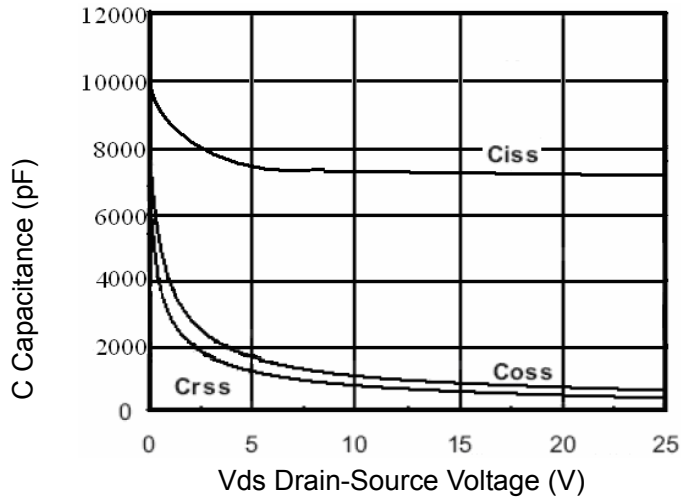


Figure 7 Capacitance vs Vds

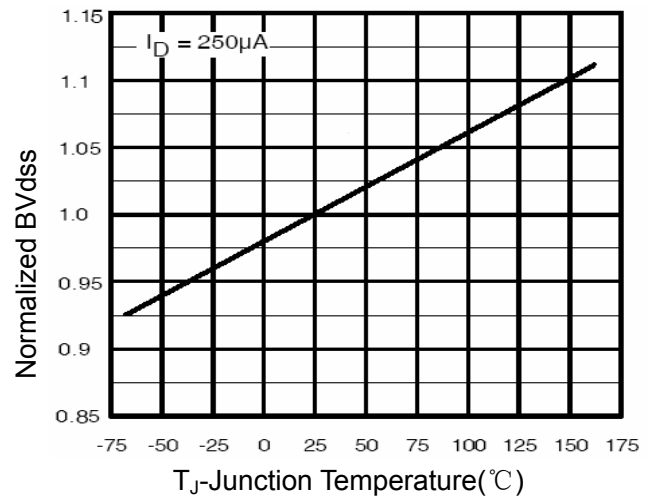


Figure 9 BV_{DSS} vs Junction Temperature

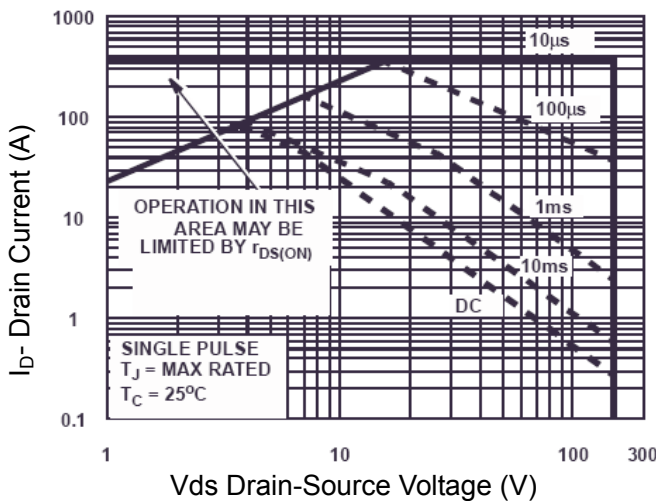


Figure 8 Safe Operation Area

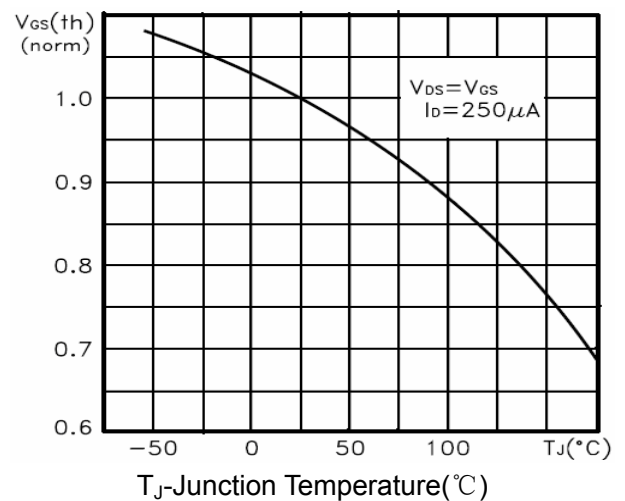


Figure 10 $V_{GS(th)}$ vs Junction Temperature

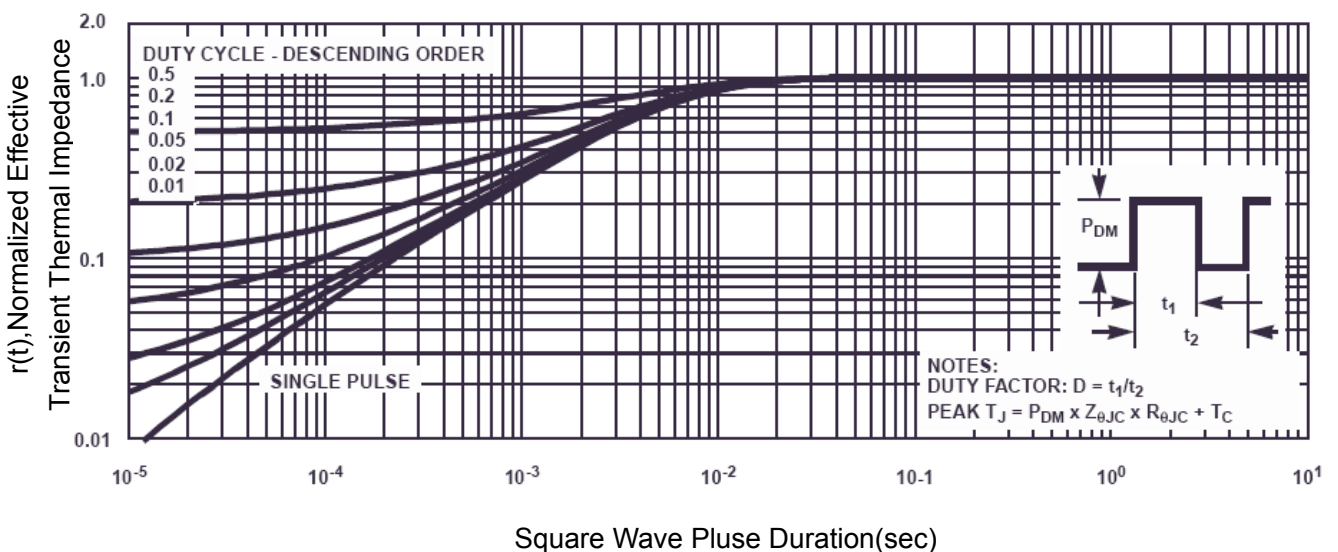
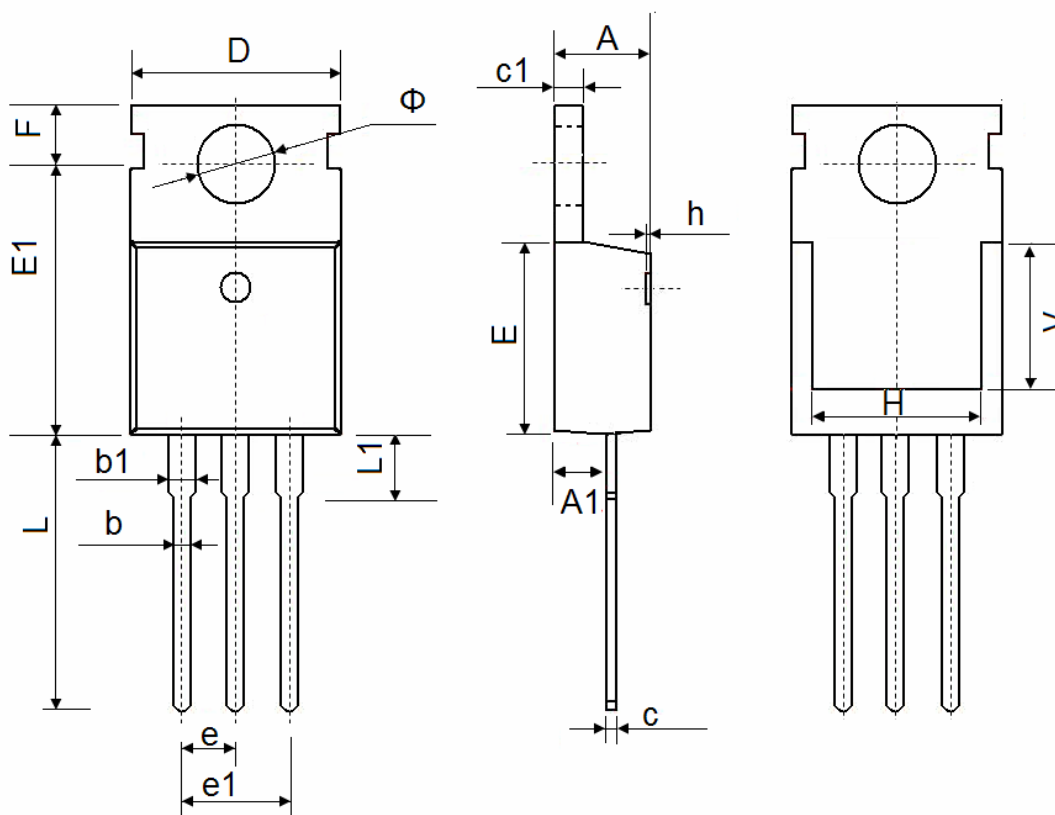


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150