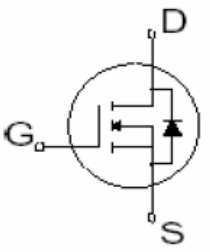
StarMOS^T Power MOSFET

- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



V_{DSS} = 500V

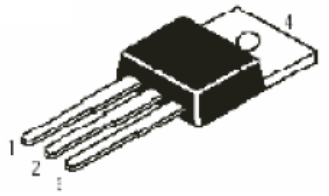
I_{D25} = 14A

$R_{DS(ON)}$ = 0.45 Ω

Description

StarMOS is a new generation of high voltage N–Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.

TO-220



Pin1–Gate
Pin2–Drain
Pin1–Source

Application

- Switching application

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D@Tc=25°C	Continuous Drain Current, V_{GS}@10V	14	A
I_D@Tc=100°C	Continuous Drain Current, V_{GS}@10V	9.1	
I_{DM}	Pulsed Drain Current ①	56	
P_D@Tc=25°C	Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy ②	560	mJ
I_{AR}	Avalanche Current ①	14	A
E_{AR}	Repetitive Avalanche Energy ①	25	mJ
dv/dt	Peak Diode Recovery dv/dt ③	9.2	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	°C
	Soldering Temperature, for 10 seconds Mounting Torque,6-32 or M3 screw	300(1.6mm from case) 10 lbf•in(1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	0.50	°C/W
$R_{\theta CS}$	Case-to-Sink,Flat,Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics @T_J=25°C(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS}=0V,I_D=250μA
$\triangle V_{(BR)DSS}/\triangle T_J$	Breakdown Voltage Temp.Coefficient	—	0.55	—	V/°C	Reference to 25°C,I_D=1mA
$R_{DS(on)}$	Static Drain-to-Source On-resistance	—	—	0.45	Ω	V_{GS}=10V,I_D=8.4A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS},I_D=250μA
gfs	Forward Transconductance	8.1	—	—	S	V_{DS}=50V,I_D=8.4A
I_{DSS}	Drain-to-Source Leakage current	—	—	25	μA	V_{DS}=500V,V_{GS}=0V
		—	—	250		V_{DS}=400V,V_{GS}=0V,T_J=150°C
I_{GSS}	Gate-to-Source Forward leakage	—	—	100	nA	V_{GS}=30V
	Gate-to-Source Reverse leakage	—	—	-100		V_{GS}=-30V
Qg	Total Gate Charge	—	—	81	nC	I_D=14A
Qgs	Gate-to-Source charge	—	—	20		V_{DS}=400V
Qgd	Gate-to-Drain("Miller") charge	—	—	36		V_{GS}=10V
td(on)	Turn-on Delay Time	—	15	—	nS	V_{DD}=250V
tr	Rise Time	—	39	—		I_D=14A
td(off)	Turn-Off Delay Time	—	39	—		R_G=7.5Ω
tf	Fall Time	—	31	—		V_{GS} =10V
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1910	—	pF	V_{GS}=0V
Coss	Output Capacitance	—	290	—		V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance	—	11.0	—		f=1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	14	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	56		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J=25°C,I_S=14A,V_{GS}=0V ④
trr	Reverse Recovery Time	—	370	550	nS	T_J=25°C,I_F=14A
Qrr	Reverse Recovery Charge	—	4.4	6.5	nC	di/dt=100A/μs ④
ton	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by Ls + L_D)				

Notes:

① Repetitive rating;pulse width limited by max.junction temperature(see figure 11)

② L = 5.7mH, IAS = 14 A, R_G = 25Ω, Starting TJ = 25°C

③ I_{SD}≤14A,di/dt≤250A/μS,V_{DD}≤$V_{(BR)DSS}$, TJ≤25°C

④ Pulse width≤300μS; duty cycle≤2%