



## TGD N-Channel Enhancement Mode Power MOSFET

**Description**

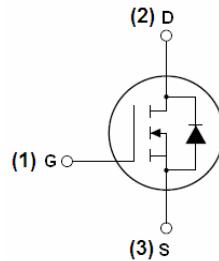
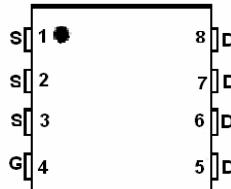
The TGD0130G uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

**General Features**

- $V_{DS} = 100V, I_D = 30A$
- $R_{DS(ON)} < 28m\Omega @ V_{GS}=10V$  (Typ:24m $\Omega$ )
- Special process technology for high ESD capability
- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation

**Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

**Schematic diagram****pin assignment****DFN5X6-8L top view****Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
0130G	0130G	DFN5X6-8L	-	-	-

**Absolute Maximum Ratings ( $T_c=25^\circ C$  unless otherwise noted)**

Symbol	Parameter	Limit	Unit
$V_{DS}$	Drain-Source Voltage	100	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current-Continuous	30	A
$I_D (100^\circ C)$	Drain Current-Continuous( $T_c=100^\circ C$ )	21	A
$I_{DM}$	Pulsed Drain Current	70	A
$P_D$	Maximum Power Dissipation	75	W
	Derating factor	0.5	W/ $^\circ C$
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	$^\circ C$

**Thermal Characteristic**

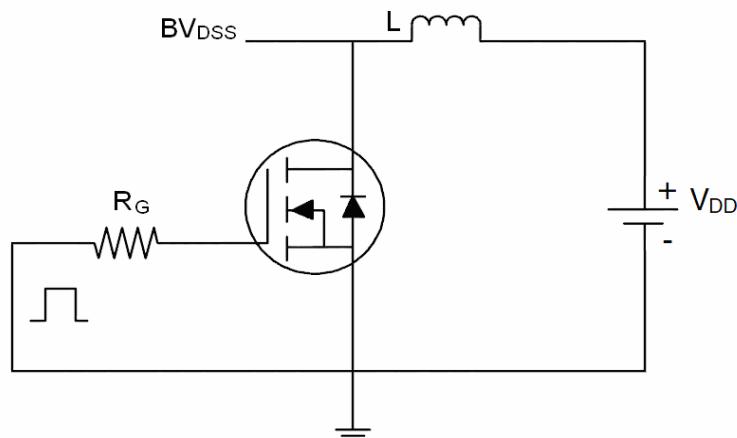
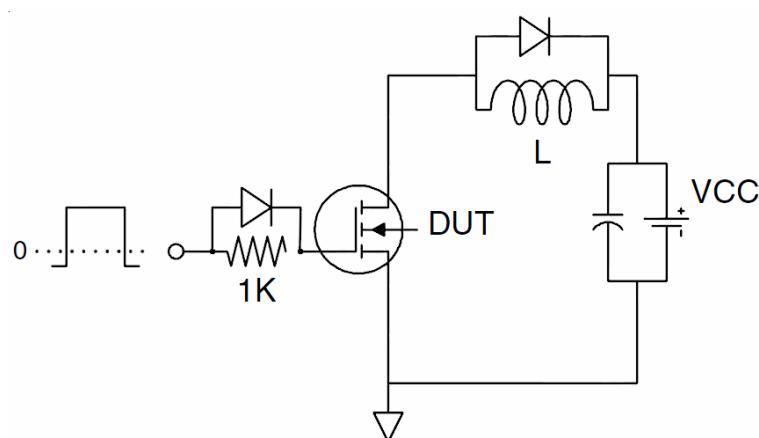
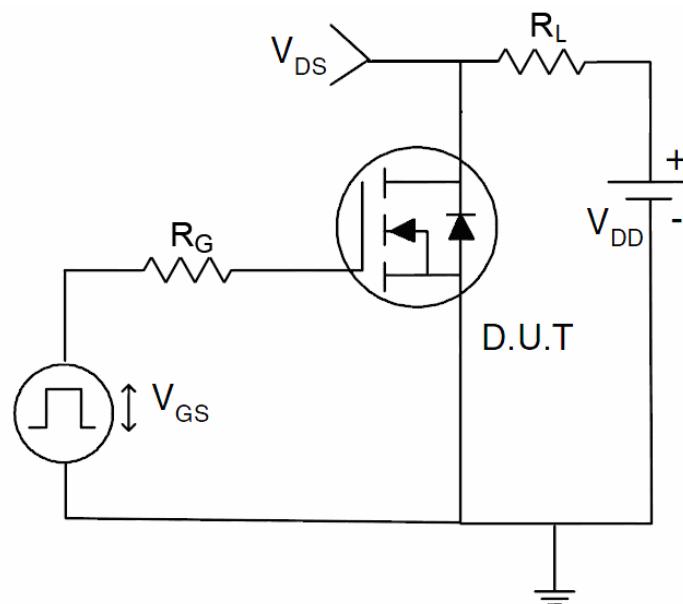
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 2)	2.0	$^\circ C/W$
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**Electrical Characteristics ( $T_C=25^\circ\text{C}$  unless otherwise noted)**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$\text{BV}_{\text{DSS}}$	Drain-Source Breakdown Voltage	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=250\mu\text{A}$	100	110	-	V
$\text{I}_{\text{DSS}}$	Zero Gate Voltage Drain Current	$\text{V}_{\text{DS}}=100\text{V}, \text{V}_{\text{GS}}=0\text{V}$	-	-	1	$\mu\text{A}$
$\text{I}_{\text{GSS}}$	Gate-Body Leakage Current	$\text{V}_{\text{GS}}=\pm 20\text{V}, \text{V}_{\text{DS}}=0\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <small>(Note 3)</small>						
$\text{V}_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$\text{V}_{\text{DS}}=\text{V}_{\text{GS}}, \text{I}_D=250\mu\text{A}$	2	3	4	V
$\text{R}_{\text{DS}(\text{ON})}$	Drain-Source On-State Resistance	$\text{V}_{\text{GS}}=10\text{V}, \text{I}_D=10\text{A}$	-	24	28	$\text{m}\Omega$
$\text{g}_{\text{FS}}$	Forward Transconductance	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=10\text{A}$	-	15	-	S
<b>Dynamic Characteristics</b> <small>(Note 4)</small>						
$\text{C}_{\text{iss}}$	Input Capacitance	$\text{V}_{\text{DS}}=25\text{V}, \text{V}_{\text{GS}}=0\text{V},$ $F=1.0\text{MHz}$	-	2000	-	PF
$\text{C}_{\text{oss}}$	Output Capacitance		-	300	-	PF
$\text{C}_{\text{rss}}$	Reverse Transfer Capacitance		-	250	-	PF
<b>Switching Characteristics</b> <small>(Note 4)</small>						
$t_{\text{d(on)}}$	Turn-on Delay Time	$\text{V}_{\text{DD}}=50\text{V}, \text{R}_{\text{L}}=5\Omega$ $\text{V}_{\text{GS}}=10\text{V}, \text{R}_{\text{GEN}}=3\Omega$	-	7	-	nS
$t_r$	Turn-on Rise Time		-	7	-	nS
$t_{\text{d(off)}}$	Turn-Off Delay Time		-	29	-	nS
$t_f$	Turn-Off Fall Time		-	7	-	nS
$Q_g$	Total Gate Charge	$\text{V}_{\text{DS}}=50\text{V}, \text{I}_D=18\text{A},$ $\text{V}_{\text{GS}}=10\text{V}$	-	39	-	nC
$Q_{\text{gs}}$	Gate-Source Charge		-	8	-	nC
$Q_{\text{gd}}$	Gate-Drain Charge		-	12	-	nC
<b>Drain-Source Diode Characteristics</b>						
$\text{V}_{\text{SD}}$	Diode Forward Voltage <small>(Note 3)</small>	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_s=20\text{A}$	-	-	1.2	V
$\text{I}_s$	Diode Forward Current <small>(Note 2)</small>	-	-	-	30	A
$t_{\text{rr}}$	Reverse Recovery Time	$\text{TJ} = 25^\circ\text{C}, \text{IF} = 18\text{A}$ $\text{di/dt} = 100\text{A}/\mu\text{s}$ <small>(Note 3)</small>	-	32	-	nS
$\text{Q}_{\text{rr}}$	Reverse Recovery Charge		-	53	-	nC
$t_{\text{on}}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

**Test Circuit****1) E<sub>AS</sub> Test Circuit****2) Gate Charge Test Circuit****3) Switch Time Test Circuit**

### Typical Electrical and Thermal Characteristics (Curves)

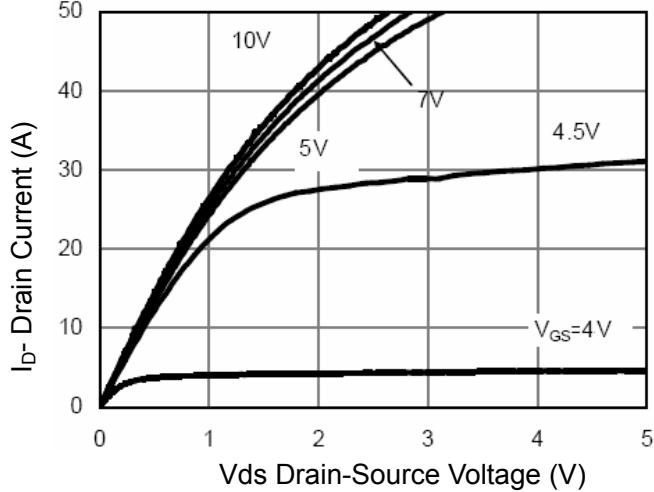


Figure 1 Output Characteristics

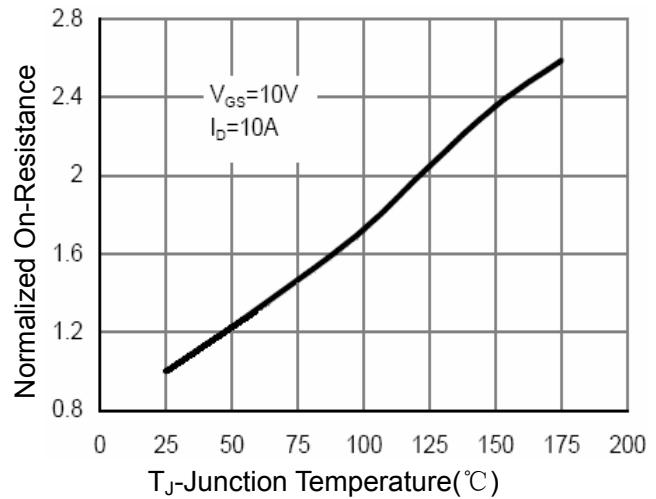


Figure 4 Rdson-JunctionTemperature

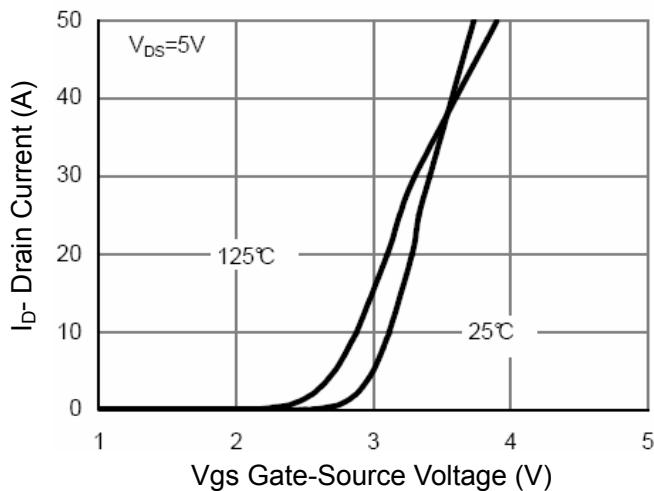


Figure 2 Transfer Characteristics

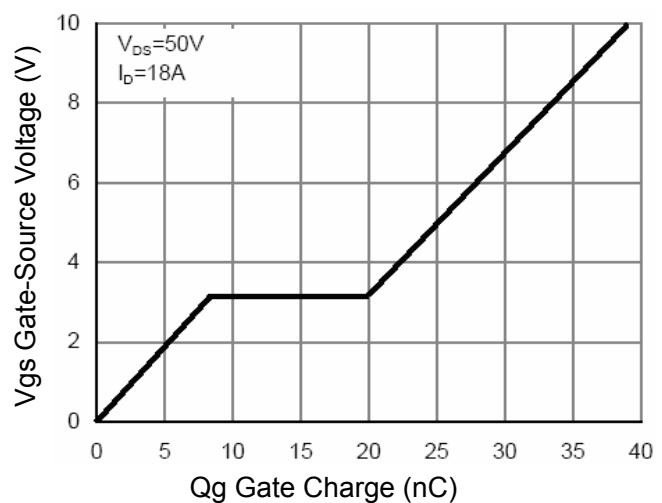


Figure 5 Gate Charge

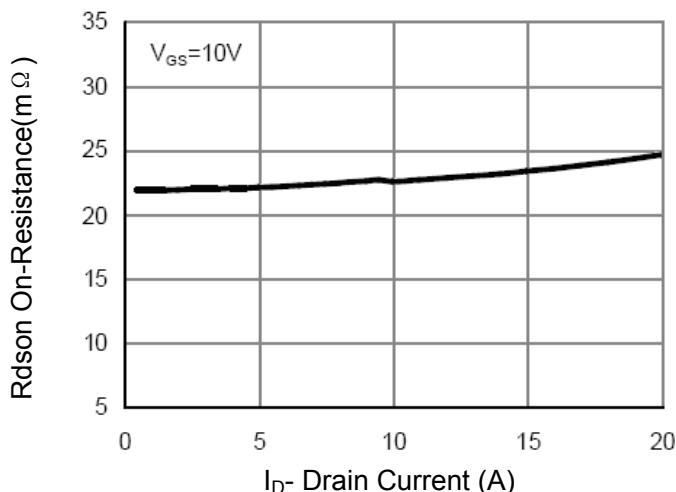


Figure 3 Rdson- Drain Current

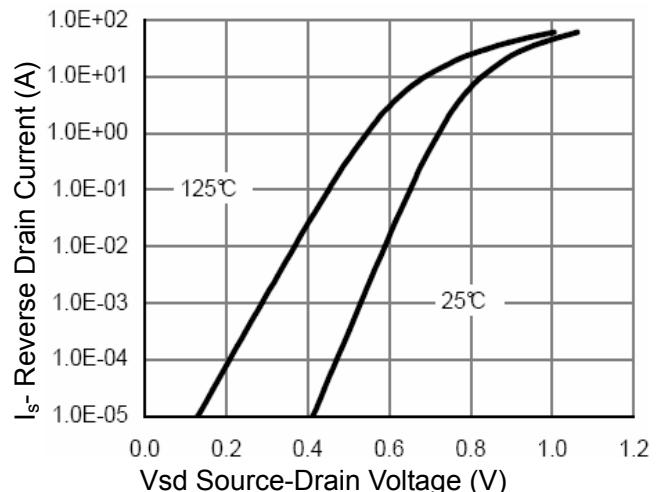
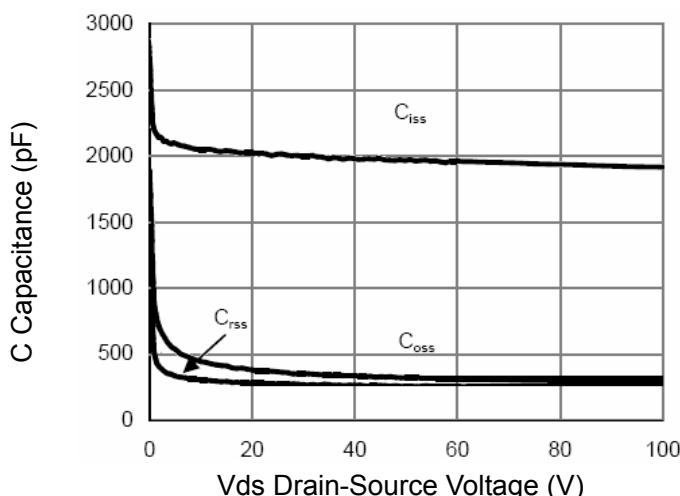
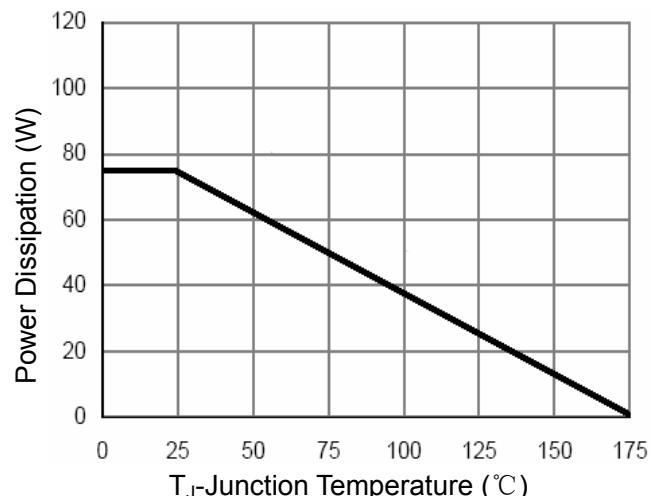


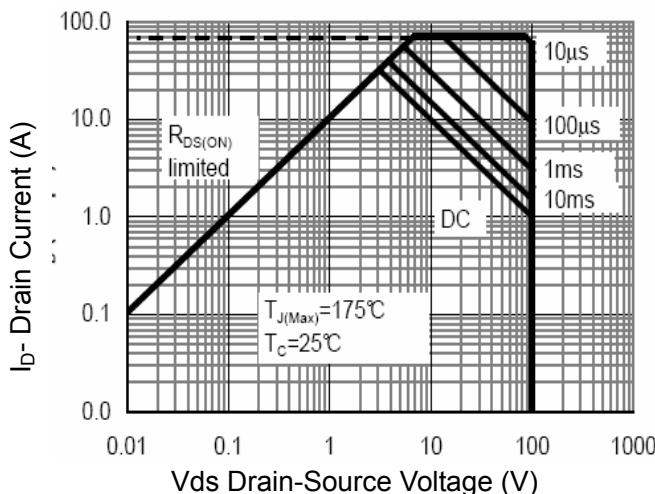
Figure 6 Source- Drain Diode Forward



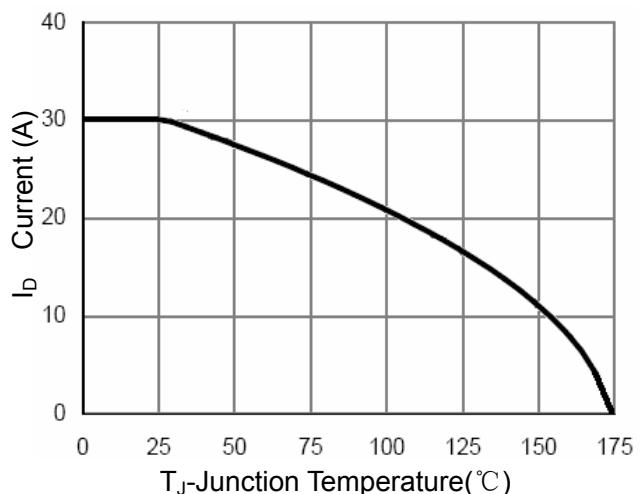
**Figure 7 Capacitance vs Vds**



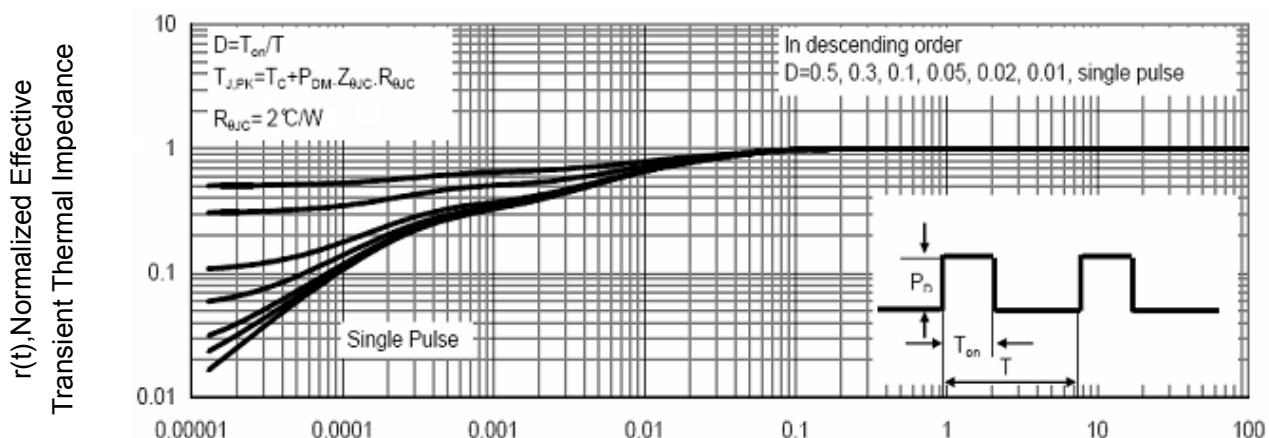
**Figure 9 Power De-rating**



**Figure 8 Safe Operation Area**



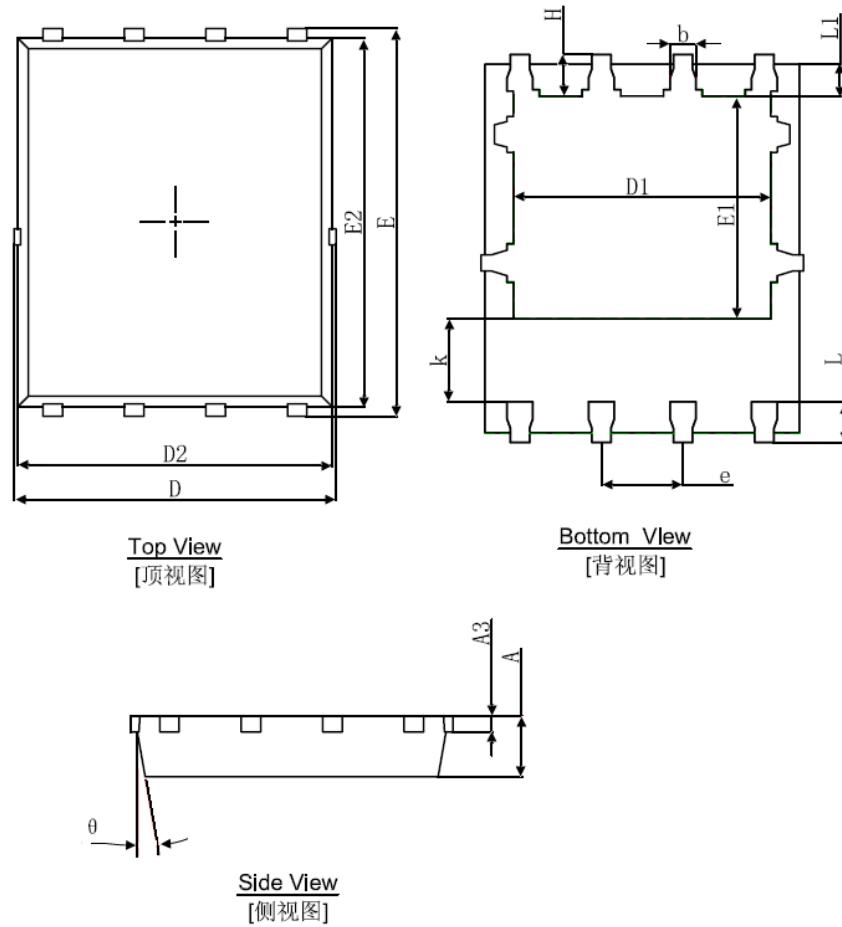
**Figure 10 ID Current- Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**



## DFN5X6-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
K	1.190	1.390	0.047	0.055
b	0.035	0.450	0.014	0.018
e	1.270(TYP.)		0.050(TYP.)	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°