



TGD N-Channel Enhancement Mode Power MOSFET

Description

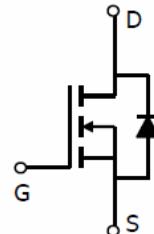
The TGD4009S uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge . The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

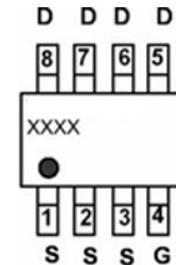
● N-Channel

 $V_{DS} = 40V, I_D = 9A$ $R_{DS(ON)} < 16m\Omega @ V_{GS}=10V$ $R_{DS(ON)} < 24m\Omega @ V_{GS}=4.5V$

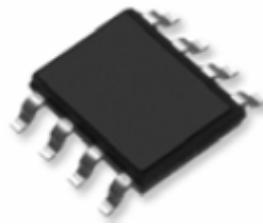
- High power and current handing capability
- Lead free product is acquired
- Surface mount package



Schematic diagram



pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TGD4009S	TGD4009S	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	9	A
Drain Current-Continuous($T_c=100^\circ C$)	$I_D (100^\circ C)$	6.4	A
Pulsed Drain Current	I_{DM}	40	A
Maximum Power Dissipation	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	62.5	°C/W
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**N-CH Electrical Characteristics ($T_A=25^\circ C$ unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=8A$	-	12.9	16	$m\Omega$
		$V_{GS}=4.5V, I_D=4A$	-	18.9	24	$m\Omega$
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=8A$	33	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=20V, V_{GS}=0V, F=1.0MHz$	-	964	-	PF
Output Capacitance	C_{oss}		-	109	-	PF
Reverse Transfer Capacitance	C_{rss}		-	96	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, R_L=2.5\Omega$ $V_{GS}=10V, R_{GEN}=3\Omega$	-	5.5	-	nS
Turn-on Rise Time	t_r		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	24	-	nS
Turn-Off Fall Time	t_f		-	12	-	nS
Total Gate Charge	Q_g	$V_{DS}=20V, I_D=8A, V_{GS}=10V$	-	22.9	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain Charge	Q_{gd}		-	5.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=9A$	-	0.8	1.2	V

N- Channel Typical Electrical and Thermal Characteristics (Curves)

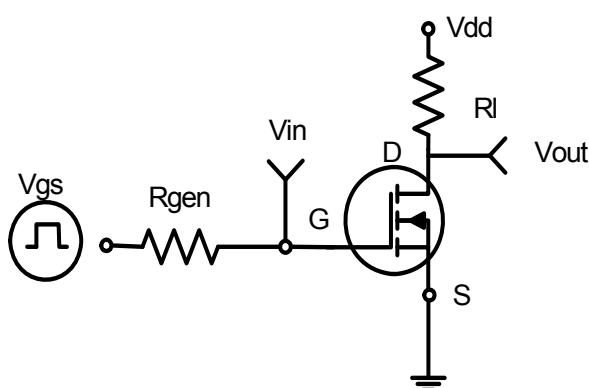


Figure 1:Switching Test Circuit

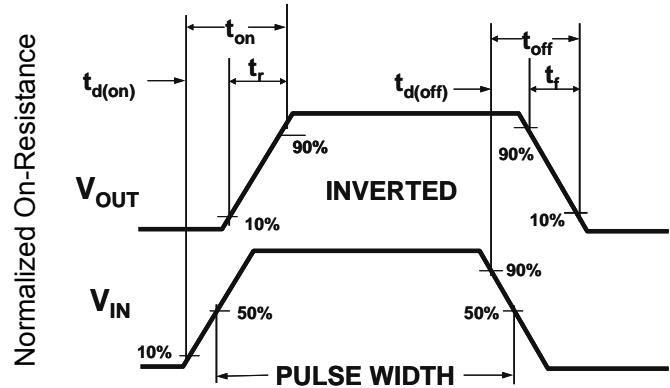


Figure 2:Switching Waveforms

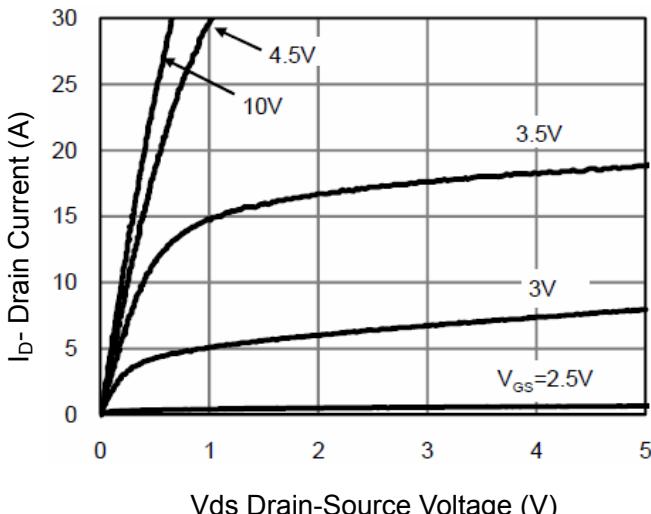


Figure 3 Output Characteristics

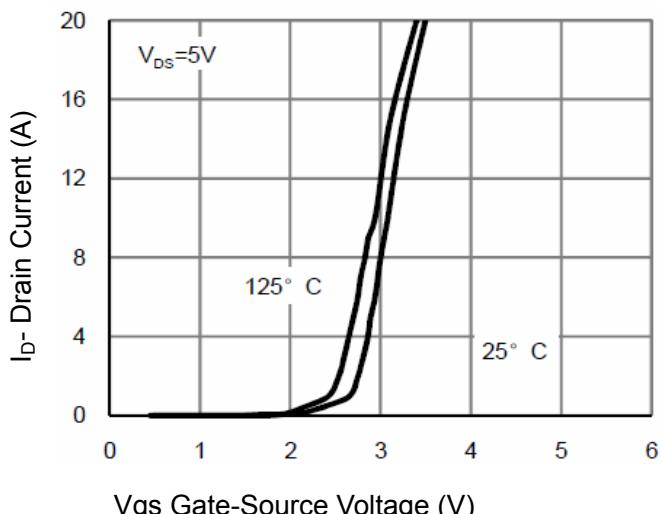


Figure 4 Transfer Characteristics

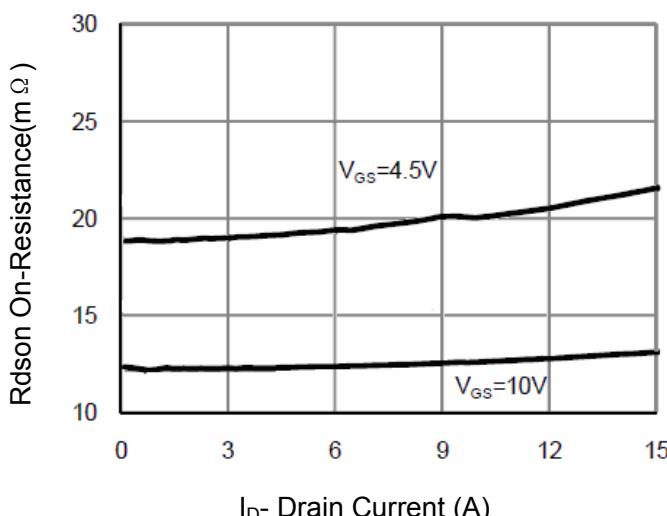


Figure 5 Drain-Source On-Resistance

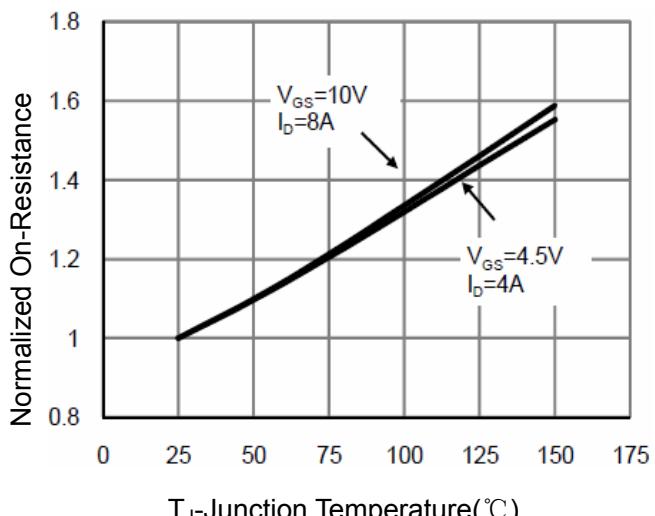
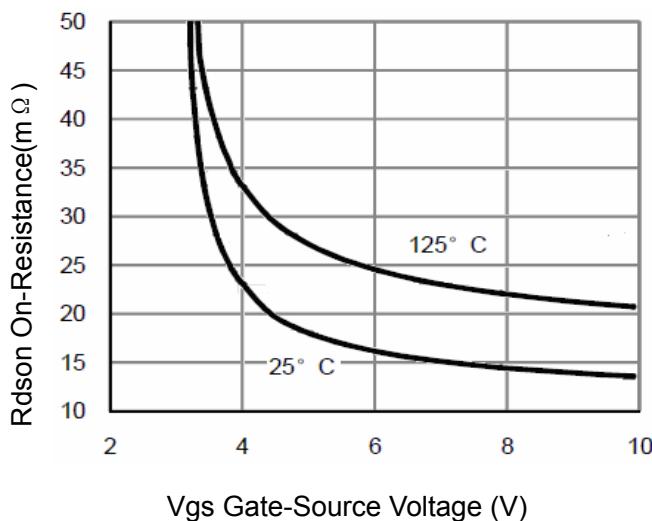
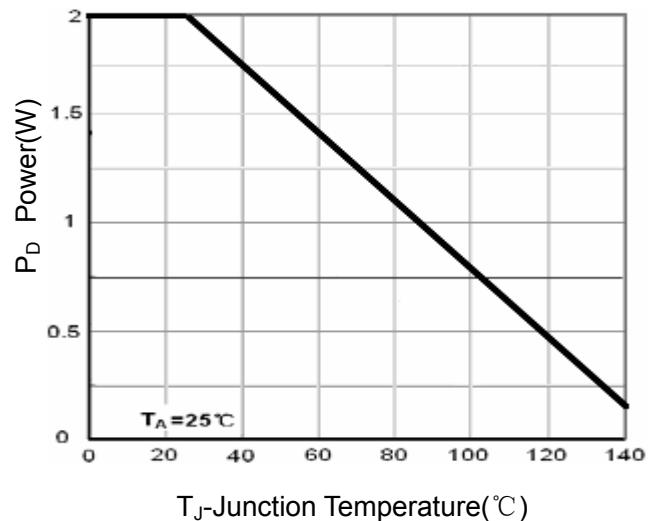


Figure 6 Drain-Source On-Resistance



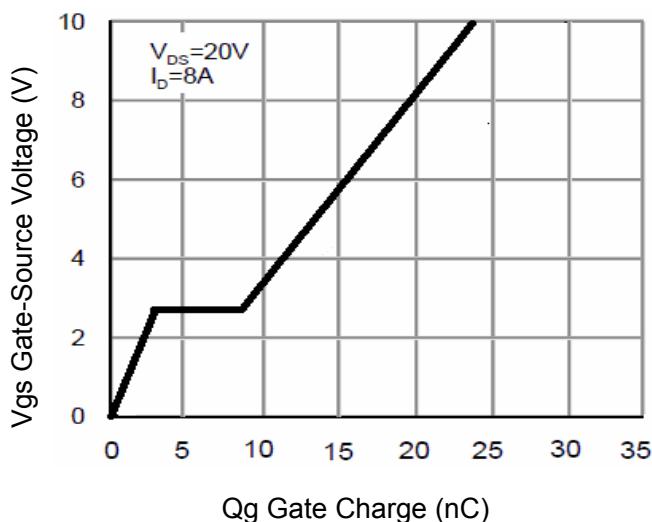
V_{GS} Gate-Source Voltage (V)

Figure 7 Rdson vs Vgs



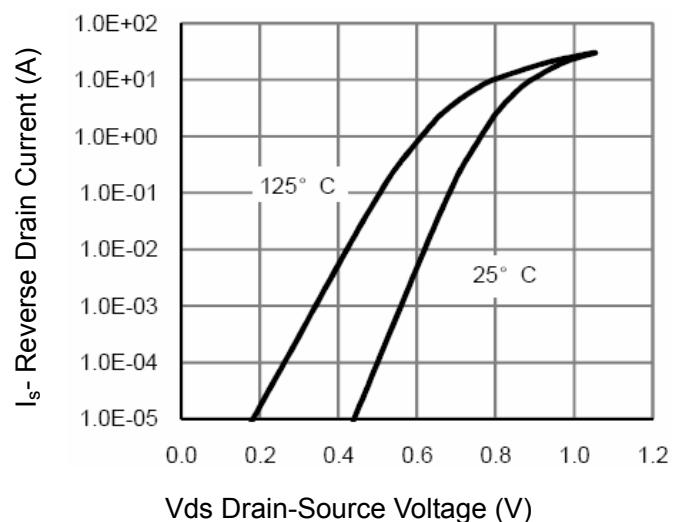
T_J -Junction Temperature(°C)

Figure 8 Power Dissipation



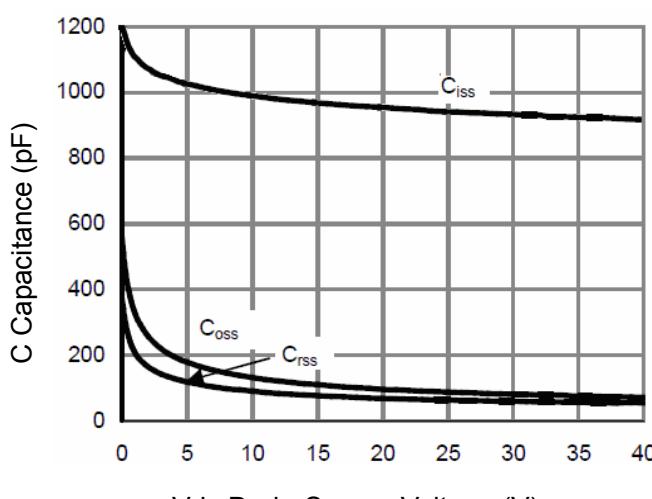
Q_g Gate Charge (nC)

Figure 9 Gate Charge



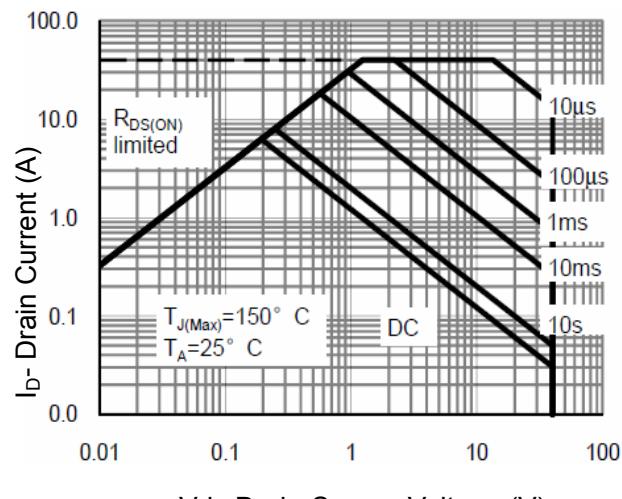
V_{DS} Drain-Source Voltage (V)

Figure 10 Source- Drain Diode Forward



V_{DS} Drain-Source Voltage (V)

Figure 11 Capacitance vs Vds



V_{DS} Drain-Source Voltage (V)

Figure 12 Safe Operation Area

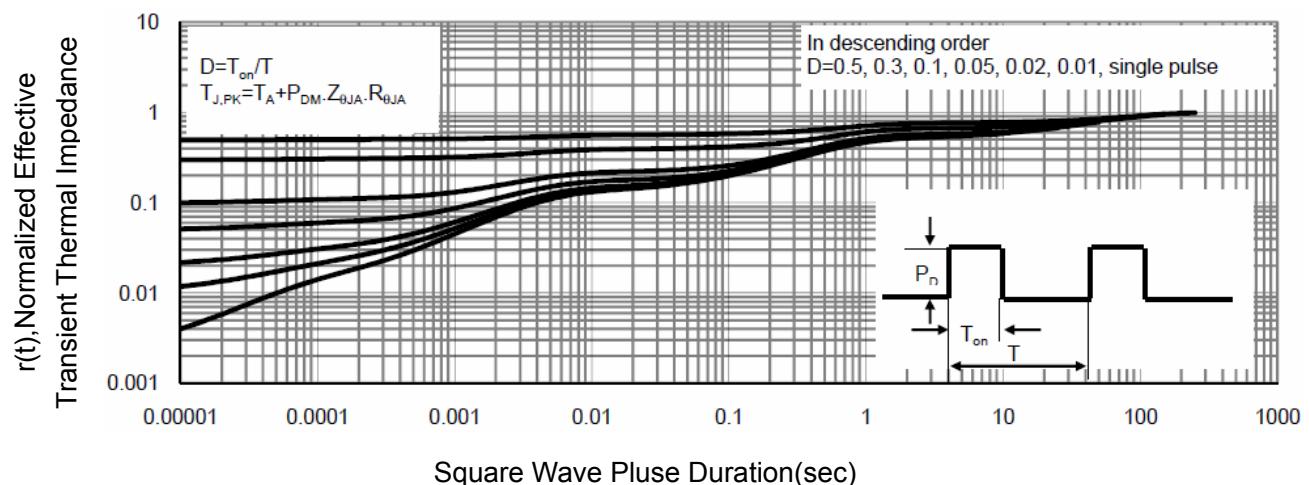
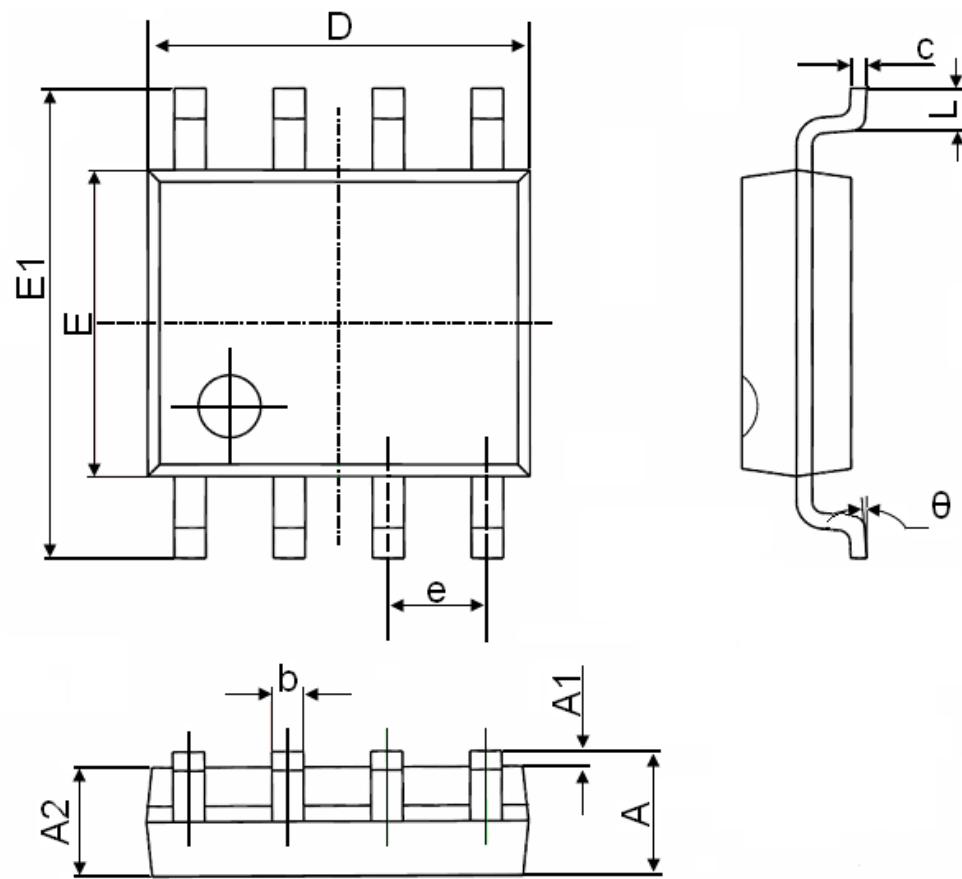


Figure 13 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°