



TGD N-Channel Enhancement Mode Power MOSFET

Description

The TGD6020I uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

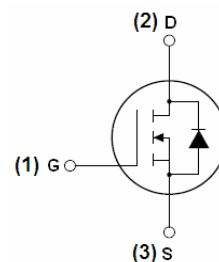
- $V_{DS} = 60V, I_D = 20A$
 $R_{DS(ON)} < 44m\Omega @ V_{GS} = 10V$
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

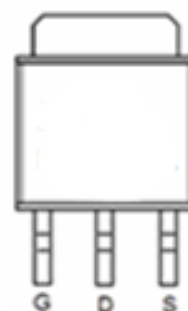
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

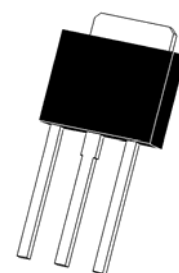
100% ΔV_{ds} TESTED!



Schematic diagram



pin assignment



TO-251 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TGD6020I	TGD6020I	TO-251	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	20	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D (100^\circ C)$	14	A
Pulsed Drain Current	I_{DM}	45	A
Maximum Power Dissipation	P_D	30	W
Derating factor		0.2	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	72	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	5	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

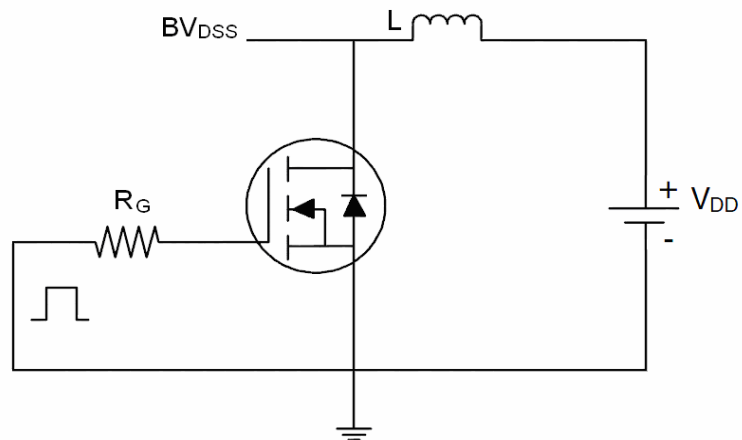
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A	-	37	44	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =4.5A	11	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	500	-	PF
Output Capacitance	C _{OSS}		-	60	-	PF
Reverse Transfer Capacitance	C _{rss}		-	25	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =2A, R _L =6.7Ω V _{GS} =10V, R _G =3Ω	-	5	-	nS
Turn-on Rise Time	t _r		-	2.6	-	nS
Turn-Off Delay Time	t _{d(off)}		-	16.1	-	nS
Turn-Off Fall Time	t _f		-	2.3	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =4.5A, V _{GS} =10V	-	14		nC
Gate-Source Charge	Q _{gs}		-	2.9		nC
Gate-Drain Charge	Q _{gd}		-	5.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	20	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =20A di/dt = 100A/μs ^(Note3)	-	35	-	nS
Reverse Recovery Charge	Q _{rr}		-	53	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

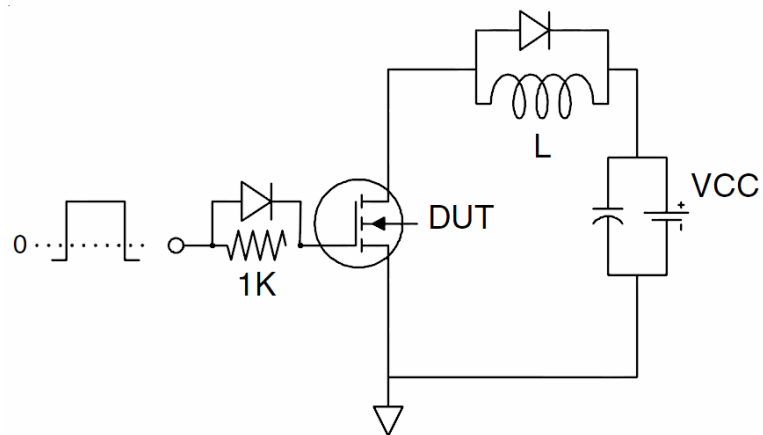
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

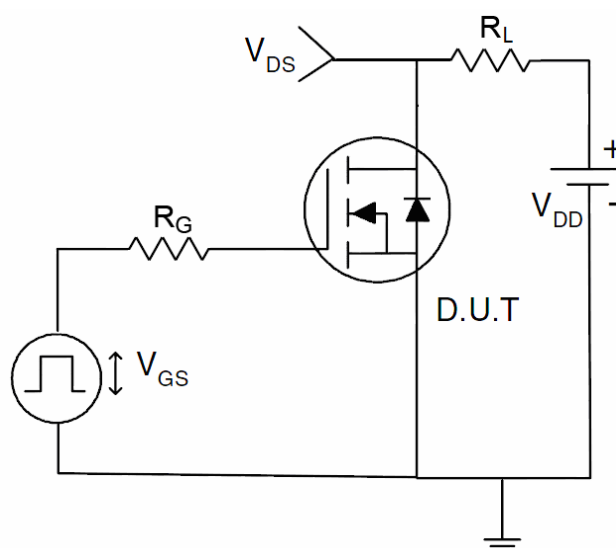
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

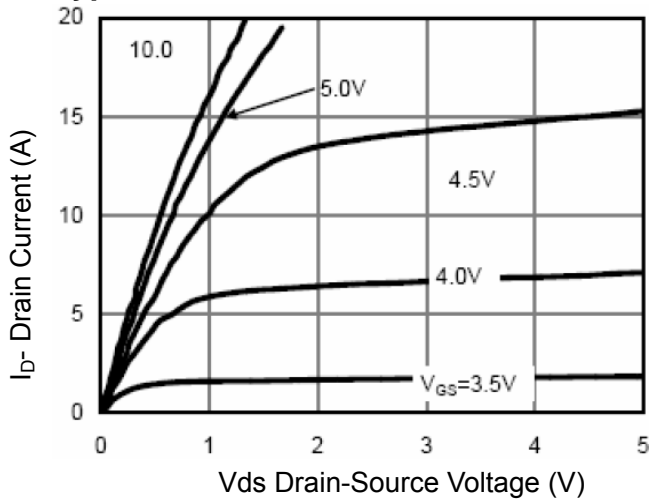


Figure 1 Output Characteristics

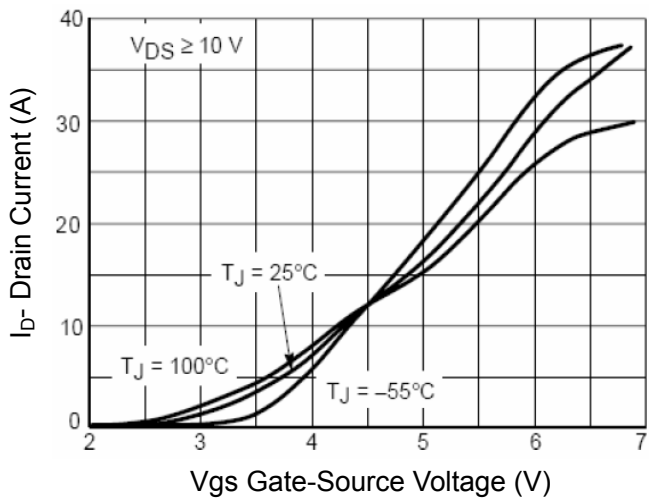


Figure 2 Transfer Characteristics

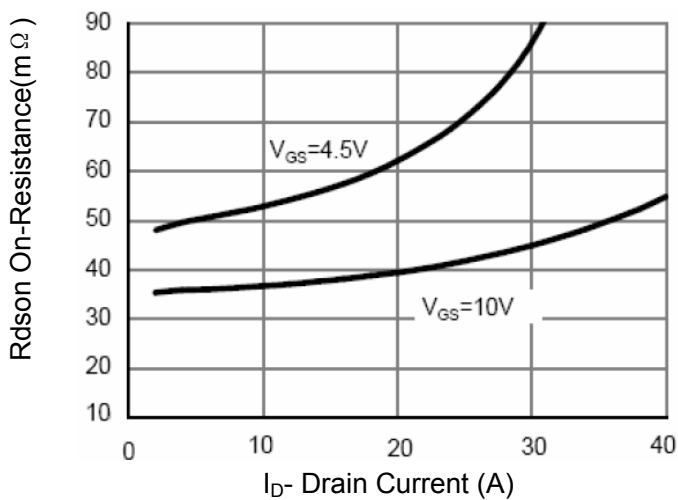


Figure 3 Rdson- Drain Current

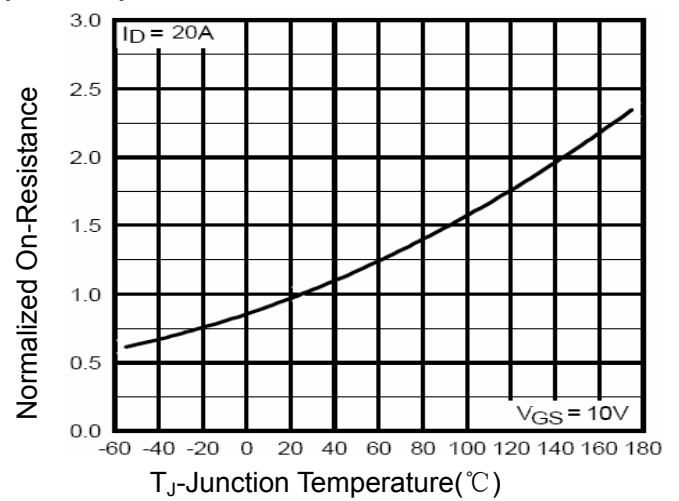


Figure 4 Rdson-Junction Temperature

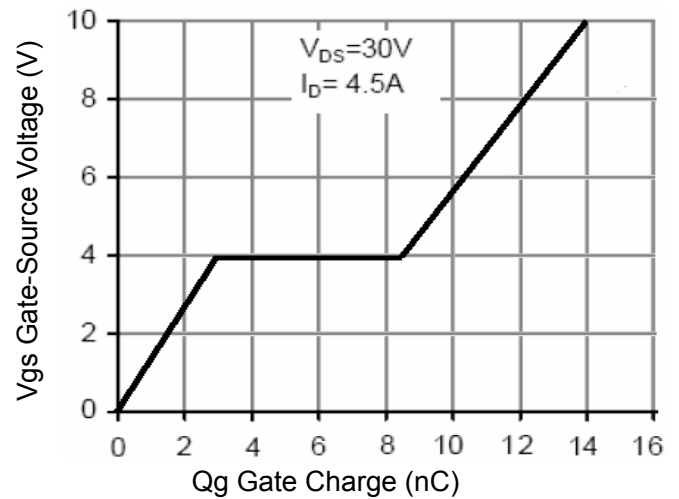


Figure 5 Gate Charge

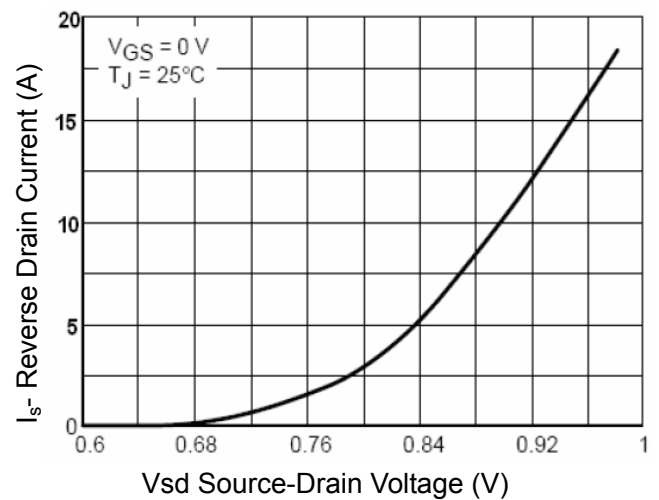


Figure 6 Source- Drain Diode Forward

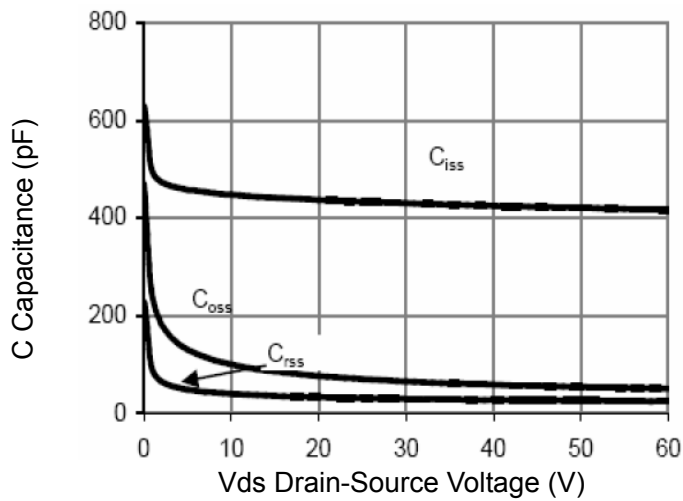


Figure 7 Capacitance vs Vds

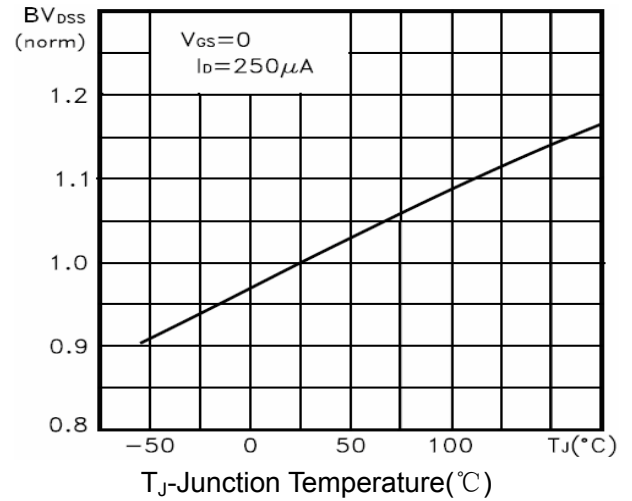
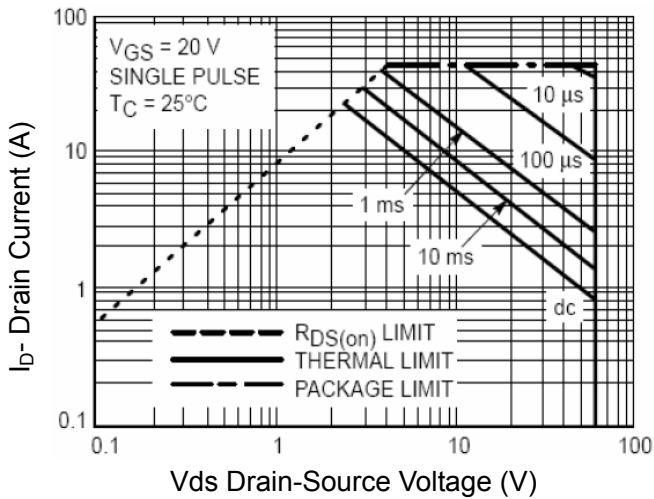

Figure 9 BV_{DSS} vs Junction Temperature


Figure 8 Safe Operation Area

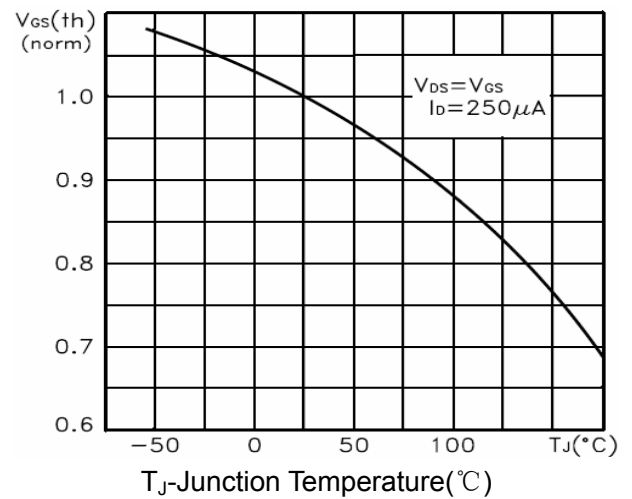
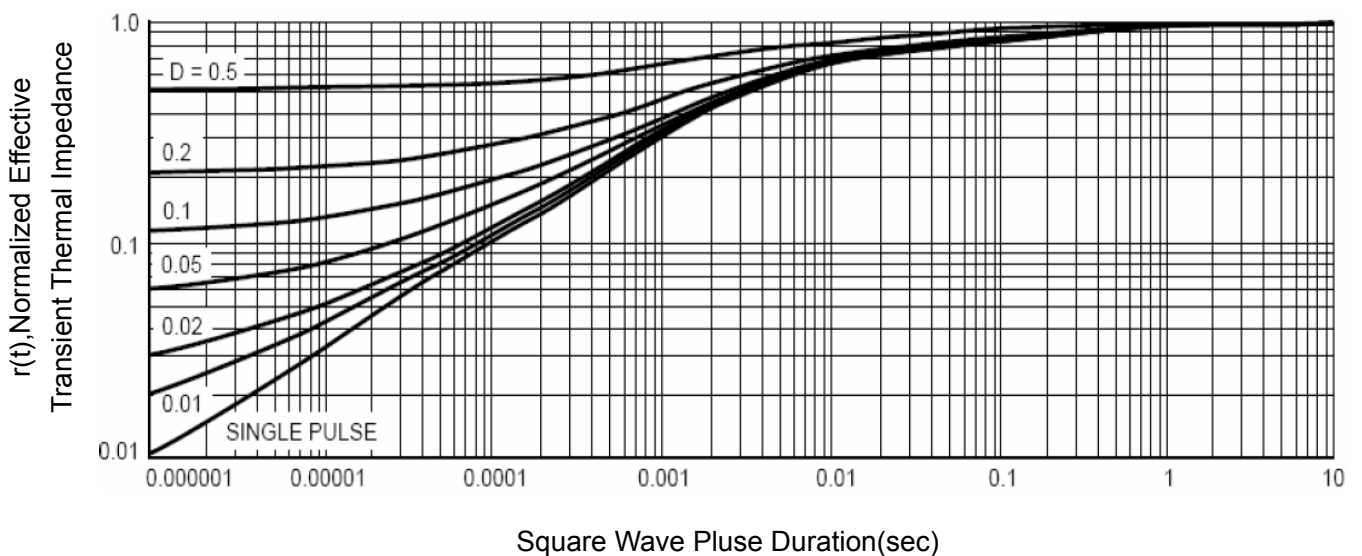
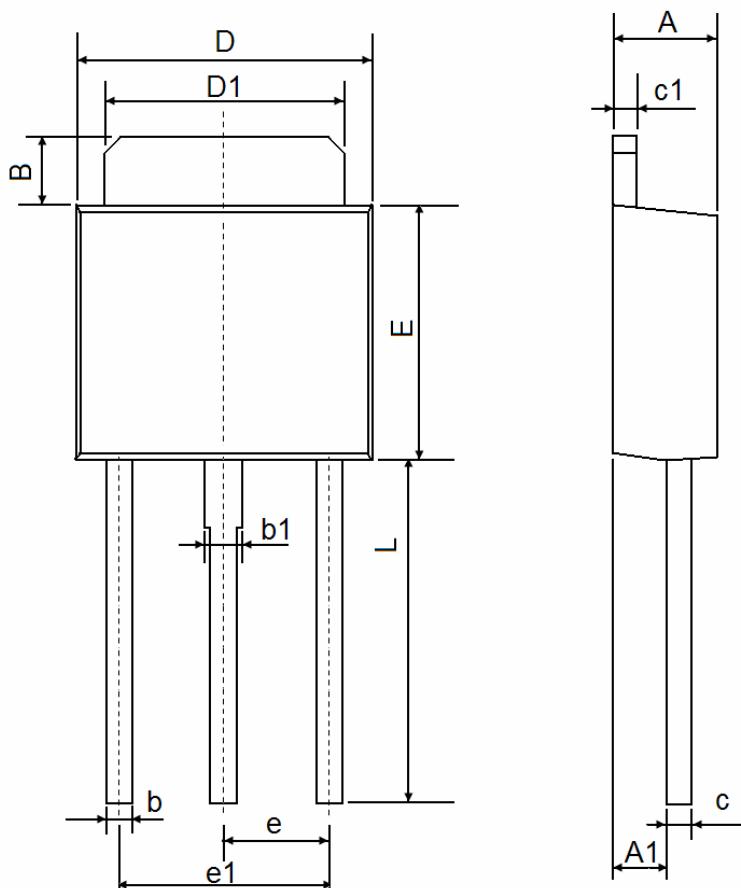

Figure 10 $V_{GS(th)}$ vs Junction Temperature


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-251 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	1.050	1.350	0.042	0.054
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP		0.091 TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311