



TGD N-Channel Enhancement Mode Power MOSFET

Description

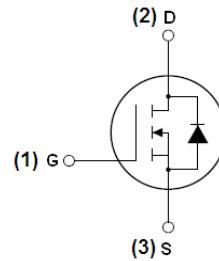
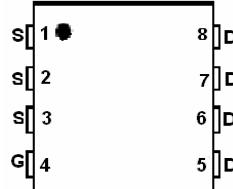
The TGD5520Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 55V, I_D = 20A$
- $R_{DS(ON)} < 22m\Omega @ V_{GS}=10V$ (Typ:19mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current

Application

- Industrial power supplies
- LED backlighting

**Schematic diagram****Pin assignment****DFN3X3 EP top view****Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
TGD5520Q	TGD5520Q	DFN3X3EP	-	-	-

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	55	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	20	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D (100^\circ C)$	14	A
Pulsed Drain Current	I_{DM}	60	A
Maximum Power Dissipation	P_D	35	W
Derating factor		0.23	W/°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	3.6	°C/W
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**Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)**

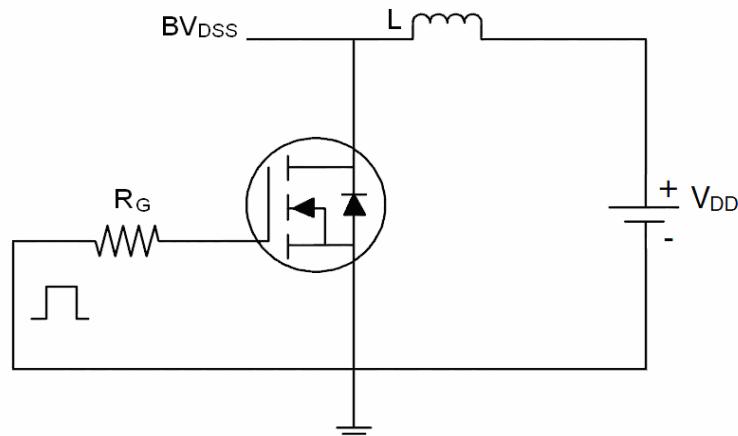
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	55		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=55\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	2	3	4	V
Drain-Source On-State Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=10\text{A}$	-	19	22	$\text{m}\Omega$
Dynamic Characteristics <small>(Note 4)</small>						
Input Capacitance	C_{iss}	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	1340	-	PF
Output Capacitance	C_{oss}		-	123	-	PF
Reverse Transfer Capacitance	C_{rss}		-	10	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DD}}=25\text{V}, I_{\text{D}}=2\text{A}, R_{\text{L}}=3\Omega, R_{\text{G}}=3\Omega$	-	6	-	nS
Turn-on Rise Time	t_{r}		-	2.5	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	22	-	nS
Turn-Off Fall Time	t_{f}		-	2.5	-	nS
Total Gate Charge	Q_{g}	$V_{\text{DS}}=25\text{V}, I_{\text{D}}=10\text{A}, V_{\text{GS}}=10\text{V}$	-	21	-	nC
Gate-Source Charge	Q_{gs}		-	5	-	nC
Gate-Drain Charge	Q_{gd}		-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{S}}=20\text{A}$	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I_{S}		-	-	20	A
Reverse Recovery Time	t_{rr}	$T_{\text{J}} = 25^\circ\text{C}, \text{IF} = 10\text{A}$ $\text{di/dt} = 100\text{A}/\mu\text{s}$ <small>(Note 3)</small>	-	16		nS
Reverse Recovery Charge	Q_{rr}		-	38		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_j=25^\circ\text{C}, V_{\text{DD}}=25\text{V}, V_{\text{G}}=10\text{V}, L=0.5\text{mH}, R_g=25\Omega$

Test circuit

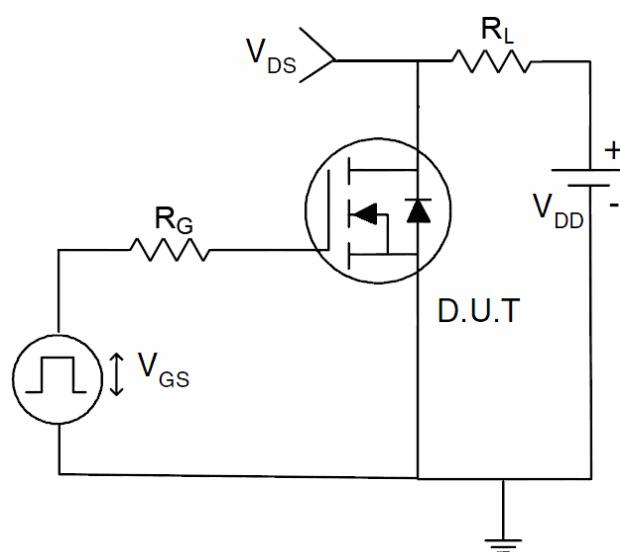
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

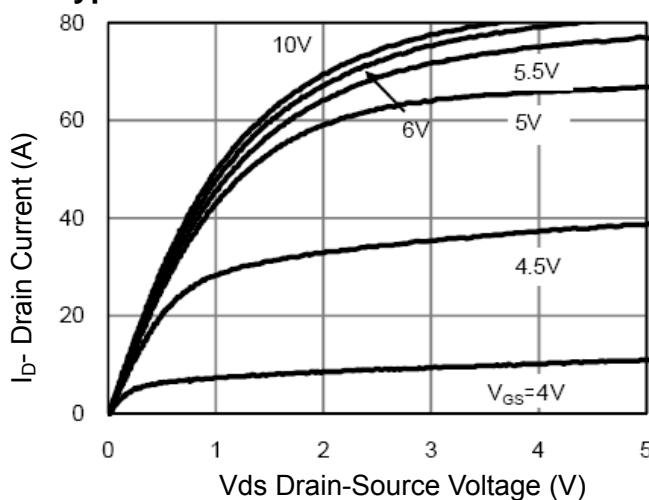


Figure 1 Output Characteristics

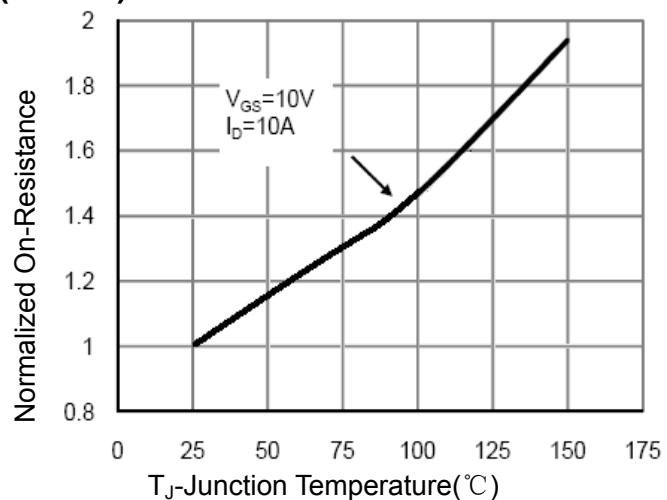


Figure 4 Rdson-JunctionTemperature

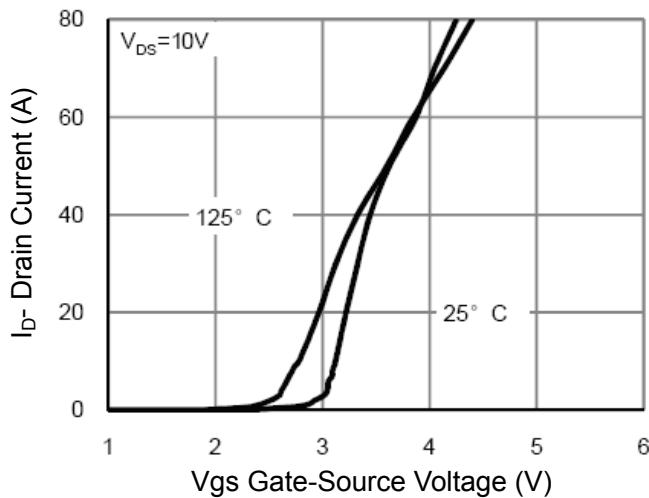


Figure 2 Transfer Characteristics

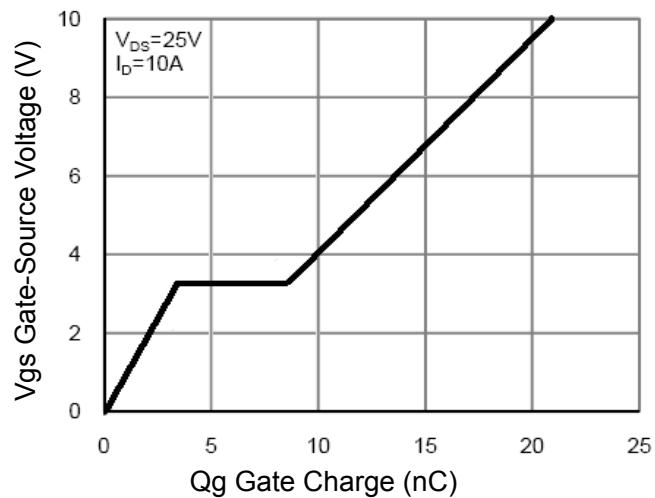


Figure 5 Gate Charge

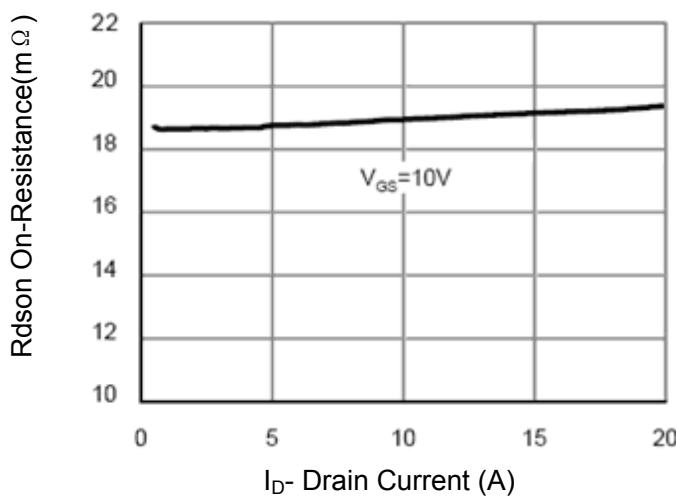


Figure 3 Rdson- Drain Current

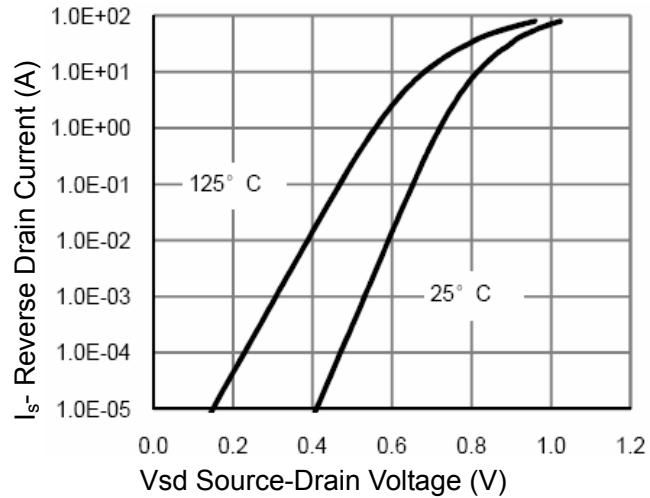


Figure 6 Source- Drain Diode Forward

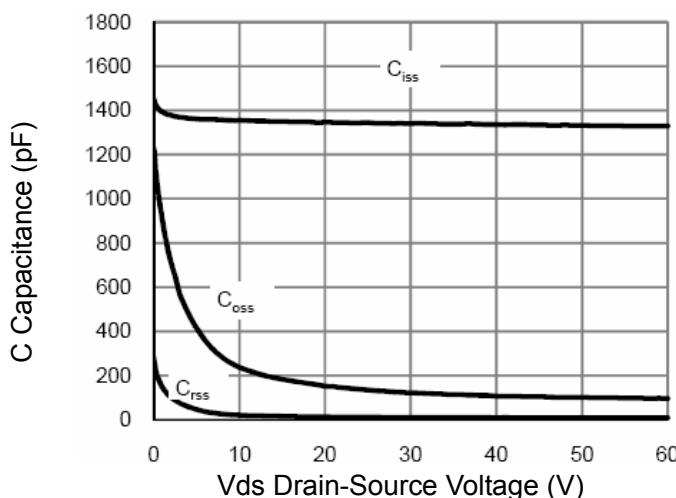


Figure 7 Capacitance vs Vds

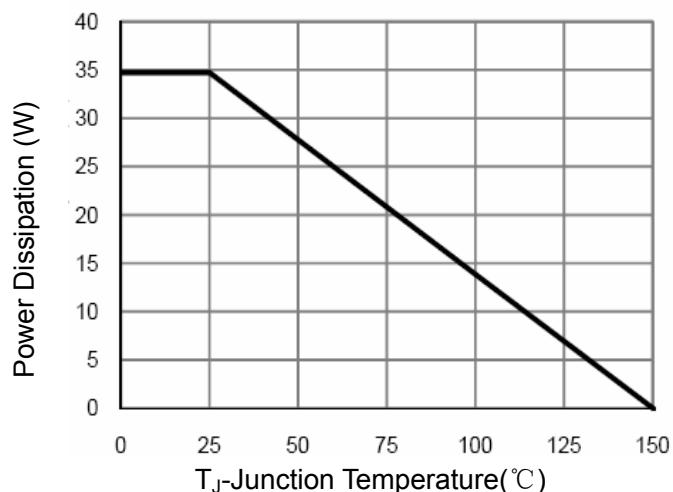


Figure 9 Power De-rating

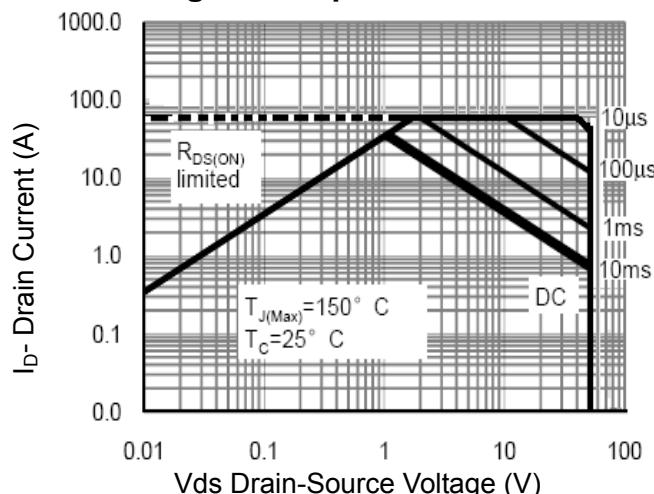


Figure 8 Safe Operation Area

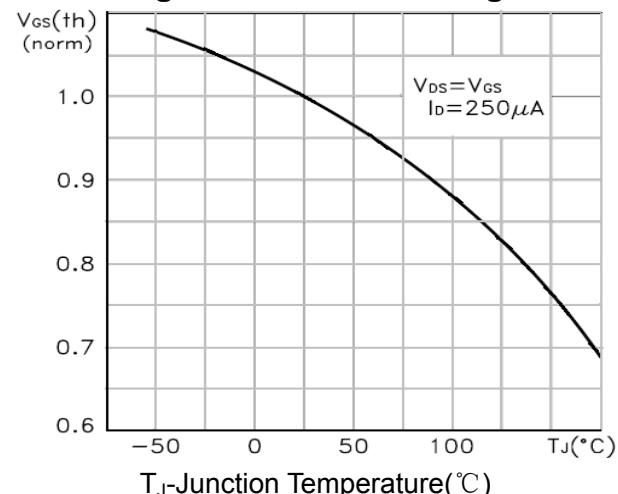


Figure 10 $V_{GS(\text{th})}$ vs Junction Temperature

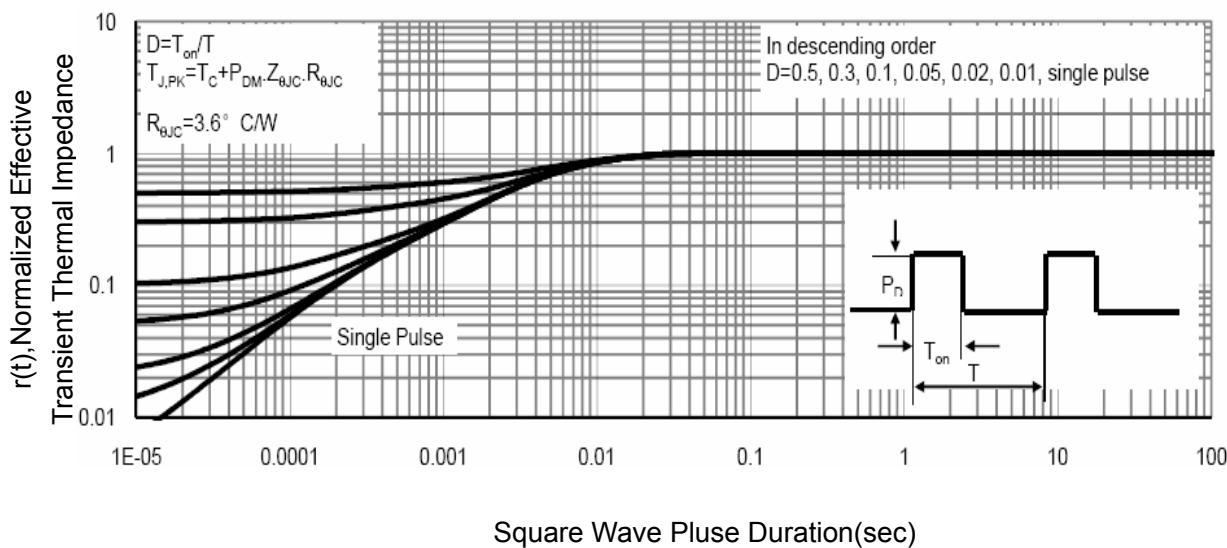
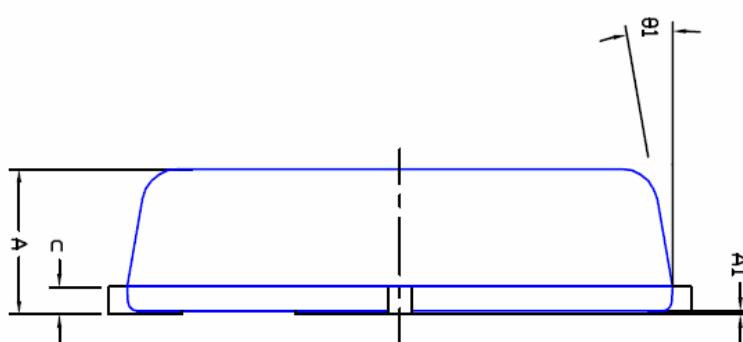
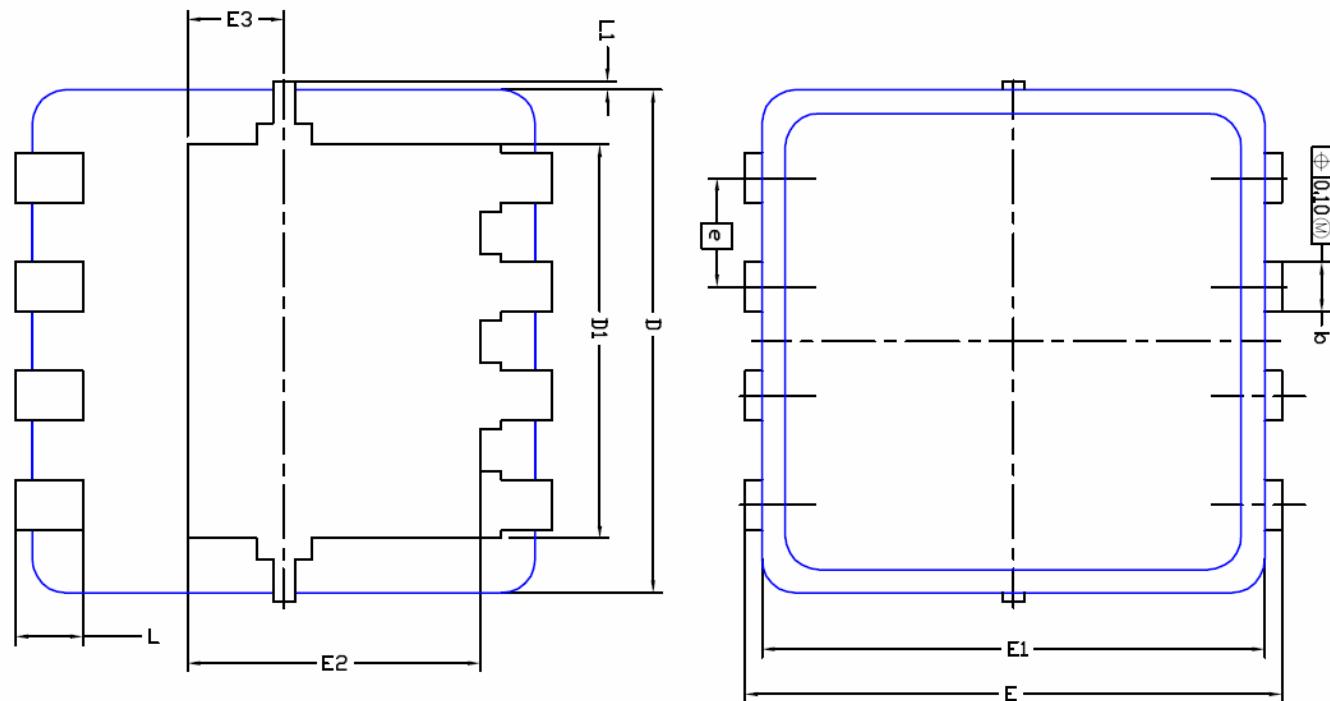


Figure 11 Normalized Maximum Transient Thermal Impedance



DFN3X3 EP Package Information



DIM.	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.80	0.900	0.0276	0.0315	0.0354
A1	0.00	---	0.05	0.000	---	0.002
b	0.24	0.30	0.35	0.009	0.012	0.014
c	0.10	0.152	0.25	0.004	0.006	0.010
D	3.00 BSC			0.118 BSC		
D1	2.35 BSC			0.093 BSC		
E	3.20 BSC			0.126 BSC		
E1	3.00 BSC			0.118 BSC		
E2	1.75 BSC			0.069 BSC		
E3	0.575 BSC			0.023 BSC		
e	0.65 BSC			0.026 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
L1	0	---	0.100	0	---	0.004
theta	0°	10°	12°	0°	10°	12°